035-17889-000
SHEET 1 OF 2
REV. F

ELEMENTARY WIRING DIAGRAM

Term 1-12 & 12-2 = 5-7 ohms
Term 12-1 & 2-12 = INF ohms

Term 3-1= 5-7 ohm
Term 1-3 = INF
Term 1-2 = INF
Term 2-1 = INF

J1-1 - J2-1 = 150K ohms
J1-2 - J2-2 = 150K ohms
J1-3 - J2-3 = 150K ohms

J1, J2, J3 unplugged 13 - 18 Ohms

J4-1= +5vdc
J4-2=+5vdc normal
J4-3=logic low run
J4-4
J4-5=+7.5vac

Phase loss
Precharge

J5 1-2= 125vac
J6 1-2= 24vac

Power supply voltages
TP- F = 12.5 vdc
TP- G = 12.8vdc
TP- A = 23 vdc

J7 5-6= 5vdc drive IGBT
J7 7-8= 5vdc filter IGBT

J4-1 = Precharge
J4-2 = 115vac in
J43 = Run

J3-5 = 1DCCT Sig
J3-6 = 1DCCT +15vdc
J3-6 = 1DCCT -15vdc
J3-10 = 2DCCT Sig
J3-11 = 2DCCT +15vdc
J3-12 = 2DCCT -15vdc

J1-3 = +15vdc
J1-4 = +5vdc
J1-5 = -5vdc
J1-6 = -15vdc
J1-7 = GND
J1-9 = fault = 0vdc
J1-12 run enable

J1-1 = 1CT 1X
J1-2 = 1CT 2X
J1-3 = 2CT 1X
J1-4 = 2CT 2X
J1-5 = 3CT 1X
J1-6 = 3CT 2X

J6-1= +5vdc +5vdc
J6-2= +5vdc normal Phase loss
J6-3= logic low run Precharge
J6-4 SCR trigger in
J6-5= +7.5vac Precharge

J3-1 neg DC bus
J3-2 center DC bus
J3-3 pos DC bus
J3-1 to neg bus 150K ohms
J3-2 to center bus 150K ohms
J3-3 to pos bus 150K ohm

TPA = logic HI run
TPB = logic low pump run
TPC=+15vdc
TPD = +10vdc
TPE = +5vdc
TPF = +7.5vdc
TPG =-15vdc
TPH = GND
TPJ = +3.3vdc
TPK = +2.5vdc

J12-1 = 115vdc power in
J12-2 = 115vac cooling pumps and fans
J12-3 = 115vac from OptiView
J12-4 = 115vac to OptiView normal VSD fault
J12-5 = 115vac VSD run command from OptiView 5 Sec of network command
J12-6 = neutral

J5 pin 1 to 2 = 5.2vdc
J5 pin 3 to 2 = 5.2vdc
J5 pin 1 to 3 = 5.2vdc
J5 pin 4 = GND

TABLE 1

UNIT STYLE	FUSING - IFU, 2FU, 3FU
YT / YS	5A, 500V, FERRAZ-SHAUMUT ATQ-5
YK	7A, 500V, FERRAZ-SHAUMUT ATQ-7

TABLE 2
LOGIC BOARD - J8, J9, J10 PINOUT

CONNECTOR PIN	FUNCTION
1	FAULT
2	GND/SHLD
3	+5V
4	UPPER PHASE
5	LOWER PHASE
6	SW. +7.5V
7	GND/SHLD

NOTE: GND/SHLD NOT CONNECTED AT DRIVER CONTROL END

TABLE 3
LOGIC BOARD - J6 PINOUT

CONNECTOR PIN	FUNCTION
1	+5V FEED
2	PH LOSS OUT
3	PRECHG IN
4	SCRTRIG IN
5	+7.5V FEED

TABLE 4
OPTIONAL HARMONIC FILTER LOGIC BOARD - J3 PINOUT

CONNECTOR PIN	IDENTIFIER	FUNCTION
1	552	TO 6T-X2 - OPTION
2	551	TO 6T-X1 - OPTION
3	554	TO 7T-X2 - OPTION
4	553	TO 7T-X1 - OPTION
5	WHITE	TO 1DCCT - OPTION
6	RED	TO 1DCCT - OPTION
7	BLK	TO 1DCCT - OPTION
8	-	TO J3 PIN 9
9	-	TO J3 PIN 8
10	RED	TO 2DCCT - OPTION
11	BLK	TO 2DCCT - OPTION
12	WHITE	TO 2DCCT - OPTION

TABLE 5
OPTIONAL HARMONIC FILTER LOGIC BOARD - J5 PINOUT

CONNECTOR PIN	IDENTIFIER	FUNCTION
1	530	TO J2-1, OPTIONAL 2022 BOARD
2	529	TO J2-2, OPTIONAL 2022 BOARD
3	528	TO J2-3, OPTIONAL 2022 BOARD
4	527	TO J2-4, OPTIONAL 2022 BOARD
5	523	TO J2-3, OPTIONAL 1624 BOARD
6	522	TO J2-2, OPTIONAL 1624 BOARD
7	521	TO J2-1, OPTIONAL 1624 BOARD
8	----	NOT USED

TABLE 6
SW3 POSITIONS

POSITION NUMBER	YORK PROTOCOL MODELS	ASCII MODBUS PROTOCOL MODELS	RTU MODBUS PROTOCOL MODELS
1	OFF	ON	ON
2	OFF	OFF	OFF
4	OFF	OFF	OFF
8	OFF	OFF	OFF
16	OFF	OFF	OFF
32	OFF	OFF	OFF
64	OFF	OFF	OFF
RTU/ASCII	OFF	ON	OFF

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