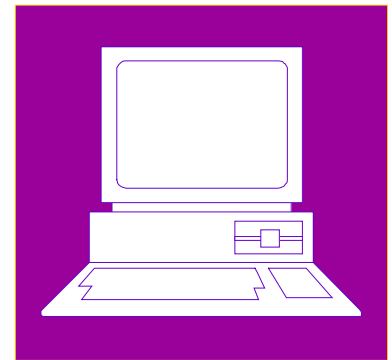
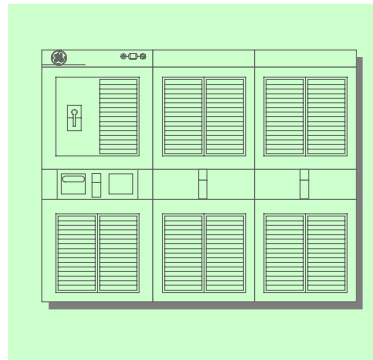
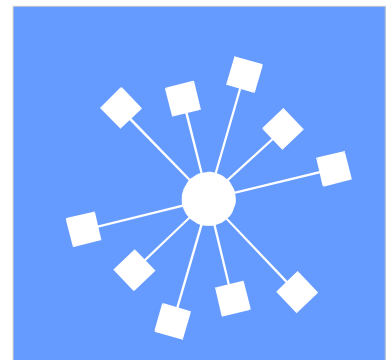




GEH-6397

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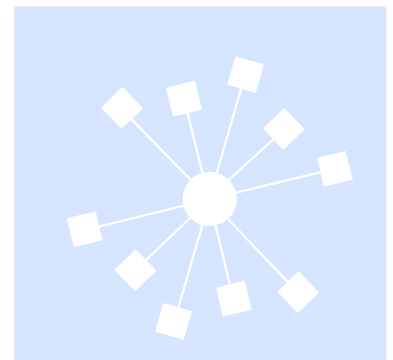


Innovation Series™

Low Voltage Drives – ACCBR-A

Reference and Troubleshooting

Publication: GEH-6397
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Innovation Series™

Low Voltage Drives – ACCBR-A

Reference and Troubleshooting

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A

Glossary

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I

Chapter 1 Faults and Troubleshooting

Introduction

The drive software includes selftest diagnostics to aid in troubleshooting. When these tests detect an unfavorable condition, they output fault indications to a display. An operator can then examine the fault and clear it, as applicable.

This chapter lists and defines the relevant fault messages for the drive, with troubleshooting suggestions. It is organized as follows:

<i>Section</i>	<i>Page</i>
Types of Faults.....	1
Fault Indication.....	2
Fault Descriptions	2

Note When troubleshooting leads to a hardware inspection or component replacement, be sure to follow the procedures described in the drive *User's Guide*, GEH-6392.



This equipment contains a potential hazard of electric shock or burn. Only adequately trained persons who are thoroughly familiar with the equipment and the instructions should maintain this equipment.

Types of Faults

Most faults can be cleared by selecting Clear Faults on the keypad or in the control system toolbox.

There are currently two types of fault conditions:

- **Trip faults** indicate a more serious condition that needs to be corrected, or it will trip the drive. The condition should be corrected before the drive is restarted.
- **Alarm faults** indicate conditions that should be noted, but that are not serious enough to shut down or trip the drive. Some alarm faults can clear themselves if

the condition goes away. Otherwise, the drive must be stopped for an operator to clear this type of fault.

Fault Indication

When a fault condition occurs, the drive displays an indicator on the two operator interfaces: the local keypad and a connected PC running the control system toolbox.

On the keypad, a fault symbol  is found on the right side of the display:

- Not flashing (on steady) indicates an alarm.
- Flashing indicates a fault.

The operator can then use the keypad to access the fault/alarm description and clear the fault (see Section 6 for details).

The **control system toolbox** uses a Windows®-based PC display. When a fault occurs, the word *Alarm* or *Trip* appears in the lower right corner of the screen. You can view a description and clear the fault using the toolbox functions. (GE publication GEH-6401 describes these tools and this feature.)

Fault Descriptions

A fault is identified by an assigned **number** and abbreviated **description**. Both of these are displayed when an operator examines a fault using the keypad or the control system toolbox. The figure shows a sample keypad display.

The table lists the drive faults and their probable cause.

Fault No.	Fault Type	Description	Alarm Indicator
ACTIVE FAULT DISPLAY			
50	Trip	HtSink temp low, B	
108	Brief	DC bus voltage low	
12	Trip	Gnd flt, coarse	
113	Trip	Invalid board set	
--- RESET FAULTS NOW ---			

Fault Display Screen on Keypad

Fault Code Descriptions

No.	Name	Type	Description
2	<i>Illegal seq state</i>	Trip	The <i>Illegal seq state</i> trip fault occurs when the sequencer state (variable <i>Sequencer state</i>) is unrecognized. This trip may occur during system development, but should not occur in the field.
6	<i>Run cmd during init</i>	Alarm	The <i>Run cmd during init</i> alarm occurs when a run request is issued during drive initialization. When the alarm occurs, the request to perform a drive action is ignored. Primary causes: The external application layer issues a request to perform a drive action during drive initialization. An external input (i.e. digital input) used to request a drive action was high during drive initialization.
7	<i>TOC pending</i>	Alarm	The <i>TOC pending</i> alarm occurs when one of the squared phase currents (variables <i>Ia² filtered</i> , <i>Ib² filtered</i> , and <i>Ic² filtered</i>) in the TOC detection model exceeds the TOC alarm level.
8	<i>Timed over current</i>	Trip	The <i>Timed over current</i> trip fault occurs when one of the squared phase currents (variables <i>Ia² filtered</i> , <i>Ib² filtered</i> , and <i>Ic² filtered</i>) in the TOC detection model exceeds the TOC threshold level.
9	<i>EE flash corrupted</i>	Trip	The <i>EE flash corrupted</i> trip fault occurs when the memory containing the drive parameters is determined to be bad during drive initialization. <i>EE flash corrupted</i> requires a hard reset to clear. Possible board failures: DSPX
11	<i>AC line failed</i>	Trip	The <i>ac line failed</i> trip fault occurs when the phase lock loop fails to synchronize during the start up sequence. Primary causes: The ac line is missing. There is a large ac line imbalance. There is a blown fuse.

Fault Code Descriptions

No.	Name	Type	Description
12	AC line transient	Alarm	The <i>ac line transient</i> alarm occurs as a result of significant phase lock loop error or significant phase imbalance. A phase imbalance signal is calculated by subtracting a control-calculated threshold from a filtered signal. Filtering the sum of two signals forms the filtered signal. One of these signals is the phase lock loop error, and the other is the error between the demodulated real component of line voltage and the measured magnitude of the line. The calculated threshold phase imbalance level that is computed by the control, is based on the magnitude of the input line voltage. This calculated phase imbalance threshold represents a phase imbalance of about 18% or a phase lock loop error of about 6.7 degrees. The phase imbalance signal, a result of the previously mentioned subtraction, is equal to about 18% imbalance when it becomes positive. The phase imbalance signal feeds an integrator designed to cause the <i>ac line transient</i> alarm when the threshold has been exceeded for a very short time. That amount of time is dependent upon the amount of the phase imbalance, but the alarm will occur eventually if the imbalance signal remains positive. Primary causes: - AC line disturbances. - Transient phase imbalances. - Weak control of frequency on diesel generator sets or gas turbine generator sets. - Very fast voltage magnitude changes. - Damaged reactor or transformer Possible board failures: - BPIA/BPIB - BICL - DSPX

Fault Code Descriptions

No.	Name	Type	Description
13	<i>AC line watchdog</i>	Trip	The <i>ac line watchdog</i> trip fault will occur when the <i>ac line transient</i> alarm persists for about one second. Both the trip fault and the alarm are a result of significant phase lock loop error, or significant phase imbalance. A phase imbalance signal is calculated by subtracting a control calculated threshold from a filtered signal. This is formed by filtering the sum of two signals. One of these signals is the phase lock loop error, and the other is the error between the demodulated real component of line voltage and the measured magnitude of the line. The calculated threshold phase imbalance level, computed by the control, is based on the magnitude of the input line voltage. This calculated phase imbalance threshold represents a phase imbalance of about 18%, or a phase lock loop error of about 6.7 degrees. The phase imbalance signal, a result of the previously mentioned subtraction, is equal to about 18% imbalance when it becomes positive. The phase imbalance signal feeds an integrator designed to cause the <i>ac line transient</i> alarm when the threshold has been exceeded for a very short time. That amount of time is dependent upon the amount of the phase imbalance, but the alarm will occur eventually if the imbalance signal remains positive. If the alarm persists continuously for about one second, the <i>ac line watchdog</i> trip fault will occur. Primary causes: AC line disturbances. Transient phase imbalances. Weak control of frequency on diesel generator sets or gas turbine generator sets. Very fast voltage magnitude changes. Damaged reactor or transformer Possible board failures: BPIA/BPIB BICL DSPX
14	<i>AC line rev phs seq</i>	Trip	The <i>ac line rev phs seq</i> trip fault occurs when the control senses that the rotation of the ac line is opposite of what is expected. This condition is checked only one time after the control is powered up. When the phase lock loop locks for the first time, just after the charging sequence has begun, the sign of <i>PLL frequency</i> is checked against the expected sign. The expected sign is determined by the setting of <i>Phase rotation req</i>. If Forward sequence is selected, the sign of <i>PLL frequency</i> is expected to be positive, otherwise, it must be negative. If the expected sign is not found, the trip fault is given. <i>AC line rev phs seq</i> requires a hard reset to clear. Before changing <i>Phase rotation req</i>, review the rotation of any ac cooling pumps or blowers in the drive. Incorrect phase sequence can lead to ineffective air or water flow in the cooling system. Primary causes: Control senses wrong phase sequence. Possible board failures: BPIA/BPIB BICL DSPX Possible wiring faults: Main ac input lines to source are not in correct phase sequence. Sensing wires to BPIA/BPIB are in wrong sequence.

Fault Code Descriptions

No.	Name	Type	Description
16	<i>Regulator in limit</i>	Alarm	The <i>Regulator in limit</i> alarm occurs when a clamp restricts one or more of several regulator outputs. This alarm will occur even if a limit is hit for a very brief period of time. The variable <i>Reg limit summary</i> stores the summary of all regulator limit bits the last time any regulator was in limit. This is a good way to see what limit caused the alarm. A list of the bit numbers for specific regulator limit flags that are part of <i>Reg limit summary</i> given below. Phase lock loop regulator: Maximum frequency limit -- bit 0 Minimum frequency limit -- bit 1 Voltage regulator: X-axis current command output in maximum limit -- bit 2 X-axis current command output in minimum limit -- bit 3 Current regulator: Bits 8 and 10 set or only bit 10 if spillover disabled --bit 4 Bits 9 and 11 set or only bit 11 if spillover disabled -- bit 5 Y-channel up/down command in maximum limit -- bit 6 Y-channel up/down command in minimum limit -- bit 7 Y-channel current command in maximum limit -- bit 8 Y-channel current command in minimum limit -- bit 9 X-channel up/down command in maximum limit -- bit 10 X-channel up/down command in minimum limit -- bit 11 If a particular limit is suspected, it may be checked by viewing the associated indication variable, as listed in the table below. Note that a very helpful diagram can be found at Diagrams/Contents/Ovr_Reg_Lim. Variable Description <i>PLL positive limit</i> The pll is in the maximum limit <i>PLL lower limit</i> The pll is in the minimum limit <i>Ireg X pos limit</i> The x-channel current command from the voltage regulator is in limit positive limit. <i>Ireg X neg limit</i> The x-channel current command from the voltage regulator is in negative limit. <i>Ix U/D in pos lim</i> The x-channel output of the inner current regulator is in limit positive limit. If the spillover gain is non-zero, this flag will not cause an alarm or fault even though it is active. The spillover gain will always be non-zero because of the control's calculation. <i>Ix U/D in neg lim</i> The x-channel output of the inner current regulator is in negative limit. When the spillover gain is non-zero, always the case because of the control calculation, this flag will not cause an alarm or fault even though it is active. <i>Ireg Y U/D pos limit</i> This flag is set when the y-axis current regulator modulation command is in its positive limit. <i>Ireg Y U/D neg limit</i> This flag is set when the y-axis current regulator modulation command is in its negative limit.

Fault Code Descriptions

No.	Name	Type	Description
17	<i>IOC setpt over range</i>	Trip	The <i>IOC setpt over range</i> trip fault indicates that the firmware instantaneous over-current threshold request is above the allowed limit. This limit is 2.5 times the rated current for the source. This threshold is a final value that is calculated to be 2.4 times the rated current, so this trip fault should only occur when design personnel over-ride the calculation of the threshold.
18	<i>Charge res over temp</i>	Trip	The <i>Charge res over temp</i> trip fault occurs when the charge resistor thermal model shows that one of the three charge resistor temperatures has exceeded the allowed threshold. This model runs once the charge resistor contactor (MB) has been commanded to close, and remains active until the charge resistor has opened. This trip fault indicates that one of the three charge resistors has over-heated. The trip fault occurs when the charge resistor change in temperature has exceeded the allowed threshold. The factory sets the trip fault level. The highest modeled temperature of the three charge resistors can be seen through <i>Charge res temp</i>. Primary causes: Short around charge resistor. Wrong charge resistor installed at factory. Too much total capacitance connected to the source. Source bridge has a short. Possible board failures: BPJA/BPIB DSPX Possible wiring faults: Charge resistor(s) shorted.
19	<i>Charge res temp hot</i>	Alarm	The <i>Charge res temp hot</i> trip fault occurs when the charge resistor thermal model shows that one of the three charge resistor temperatures has exceeded the allowed threshold. This model runs once the charge resistor contactor (MB) has been commanded to close and remains active until the charge resistor has opened. This alarm indicates that one of the three charge resistors has come close to the over-heated value. The alarm occurs when the charge resistor change in temperature has exceeded the allowed threshold. The factory sets the alarm turn on. The highest modeled temperature of the three charge resistors can be seen through <i>Charge res temp</i>. This alarm will go away when the highest modeled charge resistor temperature falls below the alarm turn off level. Primary causes: Short around charge resistor. Wrong charge resistor installed at factory. Too much total capacitance connected to the source. Source bridge has a short. Possible board failures: BPJA/BPIB DSPX Possible wiring faults: Charge resistor(s) shorted.
20	<i>Version mismatch</i>	Trip	The <i>Version mismatch</i> trip fault occurs at initialization when the drive pattern detects a product or version mismatch with the parameters stored in non-volatile RAM. Download parameters to fix.

Fault Code Descriptions

No.	Name	Type	Description
21	<i>Phase B cur offset</i>	Trip	The <i>Phase B cur offset</i> trip fault occurs when the phase B current offset (variable <i>Phs B current offset</i>) is too large. The current offset threshold level is 1 percent of the rated shunt current. <i>Phs B current offset</i> is the output of an automatic current offset calculation. <i>Phase B cur offset</i> evaluates phase B current feedback information collected while the power bridge is turned off, when current feedbacks should be zero. It uses the information to detect power bridge and feedback circuitry problems. Primary causes: The wire connection between the phase B SHCA card and the BPIA/BPIB card is missing or damaged. The phase B current feedback VCO on the BPIA/BPIB card is damaged. Two or more shorted IGBTs in the power bridge exist. A combination of a shorted IGBT in the power bridge and a ground in the load exists. Possible configuration faults: The specified frame size, represented by parameter <i>IPN frame size</i>, does not match the bridge. Possible board failures: SHCA BPIA/BPIB HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.
22	<i>DC link charge fail</i>	Trip	The dc link <i>charge fail</i> trip fault occurs only during the link charging sequence shortly after the run command is given. The control's sequencer gives the command for the charge contactor (MB) to close at the beginning of the link charge task. After waiting for an amount of time, calculated as a final value, the value of the dc link voltage is checked to make sure that the link charged up to at least a value that is 75% of the nominal rectified ac line voltage. The link voltage must also be greater than 80% of the peak-detected value of the ac line voltage. Primary causes: AC line voltage low. Short or partial short on bus. Possible board failures: DSPX BPIA/BPIB DSFC/DAMX Possible wiring faults: Mis-wiring between BPIA and DAMX or between BPIB and DSFC. Mis-wiring between DAMX and shunts or between DSFC and shunts.

Fault Code Descriptions

No.	Name	Type	Description
23	<i>Cont failed to close</i>	Trip	The <i>Cont failed to close</i> trip fault occurs when the control has given the command for the MA, or main contactor, to close, and has failed to sense that it actually closed after waiting for a period of time. This command to close happens just after the charge sequence has completed. This is the only time that this trip fault can occur. Primary causes: Main contactor failed. Possible board failures: DSPX BAIA ATBA Possible wiring faults: MA contactor sensing wire is loose or has fallen off.
24	<i>Cont opened</i>	Trip	The <i>Cont opened</i> trip fault occurs when the control has detected that the MA, or main contactor has opened once the source has closed it. Primary causes: Main contactor has opened. Possible board failures: DSPX BAIA ATBA Possible wiring faults: MA contactor sensing wire is loose or has fallen off.
25	<i>Local flt</i>	Trip	The <i>Local flt</i> trip fault occurs when the local permissive circuit is open, and a <i>Run request</i> is issued. Possible wiring faults: The connections to ATBA terminal board locations 8 (L115), 10 (L24), and 12 (LCOM) are missing or damaged. The connection to backplane connector J2 is missing or damaged.
26	<i>System flt</i>	Trip	The <i>System flt</i> trip fault occurs when the system permissive circuit is open and a run request is issued. Possible wiring faults: The connections to ATBA terminal board locations 2 (S115), 4 (S24), and 6 (SCOM) are missing or damaged.
27	<i>DC bus under voltage</i>	Trip	The <i>DC bus under voltage</i> trip fault occurs when the dc link voltage feedback (variable <i>DC bus voltage</i>), is too low. The under voltage threshold level is a function of the nominal dc link voltage, a function of the output line-line voltage (parameter <i>Max lineup output</i>). The fault is only declared when the drive is not in a stopped condition. For sources, the fault is only declared if the link is expected to be nominal. The main purpose of the trip fault is to detect an excessively low dc link voltage, and to respond by shutting down the bridge. Possible configuration faults: The parameter <i>Max lineup output</i>, power bridge output rated line-line voltage, is not set correctly. Possible board failures: BP1A/BP1B DSPX

Fault Code Descriptions

No.	Name	Type	Description
28	<i>Ground flt alm, LP</i>	Alarm	The <i>Ground flt alm, LP</i> alarm occurs when a large ground current is detected by the Line Protection (LPPA) Module. The alarm occurs when the LPPA ground current (variable <i>LPPA gnd cur</i>) is greater than the LPPA ground current alarm level (parameter <i>LPPA gnd flt alm</i>). <i>Ground flt alm, LP</i> clears when the LPPA ground current drops below the LPPA ground current alarm turn off level (parameter <i>LPPA gnd flt clt</i>). The alarm can be disabled by inhibiting Line Protection (LPPA) Module functionality. Set parameter <i>LPPA mode</i> equal to <i>LPPA absent</i>. Possible configuration faults: The value of the LPPA ground current alarm level, represented by parameter <i>LPPA gnd flt alm</i>, is too low. Possible board failures: LPPA ATBA BAIA DSPX
29	<i>Ground flt, LP</i>	Trip	The <i>Ground flt, LP</i> trip fault occurs when a large ground current is detected by the Line Protection (LPPA) Module. The trip fault occurs when the LPPA ground current (variable <i>LPPA gnd cur</i>) is greater than the LPPA ground current trip fault level (parameter <i>LPPA gnd flt lvl</i>). <i>Ground flt, LP</i> can be disabled by inhibiting Line Protection (LPPA) Module functionality. Set parameter <i>LPPA mode</i> equal to <i>LPPA absent</i>. Possible configuration faults: The value of the LPPA ground current fault threshold, represented by parameter <i>LPPA gnd flt lvl</i>, is too low. Possible board failures: LPPA ATBA BAIA DSPX
30	<i>AC filter fuse blown</i>	Alarm	The <i>ac filter fuse blown</i> alarm occurs when the Line Protection (LPPA) Module detects that the MOV fuse has blown. The trip fault occurs when the LPPA fuse circuit is open. <i>AC filter fuse blown</i> can be disabled by inhibiting Line Protection (LPPA) Module functionality. Set parameter <i>LPPA mode</i> equal to <i>LPPA absent</i>. Possible board failures: LPPA ATBA BAIA DSPX
31	<i>SW detected IOC</i>	Trip	The <i>SW detected IOC</i> trip fault occurs when a firmware IOC (instantaneous over-current) feature detects a current level on any of the three phases that exceeds 2.4 times the rated value of the source. This trip fault is normally disabled. It is enabled only when the retry time limit for the hardware generated IOC is set to zero. But that retry time is a final value driven by rules. Changing it generates an override. This fault detection scheme is not normally active. Primary causes: Excessive current demand on source Mis-phasing of phase lock loop

Fault Code Descriptions

No.	Name	Type	Description
32	<i>IOC phase A</i>	Trip	The <i>IOC phase A</i> trip fault is hardware generated. The trip fault occurs when the current measured by the phase A shunt exceeds the instantaneous overcurrent threshold, which is positive or negative 250 percent rated shunt current. It also occurs within 25 microseconds when the phase A current experiences a step change of 100 percent rated shunt. When either condition is detected, the power bridge IGBT gating is disabled immediately. For the ACCBR-A product, this fault comes after several re-tries. Each time firmware detects that hardware has seen the condition described above, a timer is incremented. If that timer exceeds a threshold of 10 msec, an IOC fault will be given that pass, and the phase indicated will be the last phase that met the conditions described above (phase A in this case). A severe line transient may cause this fault. Possible board failures: SHCA BPIA/BPIB BICL Possible wiring faults: Connections between BPIA/BPIB and SHCA.
33	<i>IOC phase B</i>	Trip	The <i>IOC phase B</i> trip fault is hardware generated. The trip fault occurs when the current measured by the phase B shunt exceeds the instantaneous overcurrent threshold, which is positive or negative 250 percent rated shunt current. It also occurs within 25 microseconds when the phase B current experiences a step change of 100 percent rated shunt. When either condition is detected, the power bridge IGBT gating is disabled immediately. For the ACCBR-A product, this fault comes after several re-tries. Each time firmware detects that hardware has seen the condition described above, a timer is incremented. If that timer exceeds a threshold of 10 msec, an IOC fault will be given that pass, and the phase indicated will be the last phase that met the conditions described above (phase B in this case). A severe line transient may cause this fault. Possible board failures: SHCA BPIA/BPIB BICL Possible wiring faults: Connections between BPIA/BPIB and SHCA.

Fault Code Descriptions

No.	Name	Type	Description
34	<i>IOC phase C</i>	Trip	The <i>IOC phase C</i> trip fault is hardware generated. The trip fault occurs when the current, measured by the phase C shunt, exceeds the instantaneous overcurrent threshold (positive or negative 250 percent rated shunt current). It also occurs within 25 microseconds when the phase C current experiences a step change of 100 percent rated shunt. When either condition is detected, the power bridge IGBT gating is disabled immediately. For the ACCBR-A product, this fault comes after several re-tries. Each time firmware detects that hardware has seen the condition described above, a timer is incremented. If that timer exceeds a threshold of 10 msec, an IOC fault will be given that pass, and the phase indicated will be the last phase that met the conditions described above (phase C in this case). A severe line transient may cause this fault. Possible board failures: SHCA BPIA/BPIB BICL Possible wiring faults: Connections between BPIA/BPIB and SHCA.
35	<i>IGBT AU desat</i>	Trip	The <i>IGBT AU desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase A upper IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase A upper IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase A lower IGBT is short-circuited. The phase A upper IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
36	<i>IGBT AL desat</i>	Trip	The <i>IGBT AL desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase A lower IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase A lower IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase A upper IGBT is short-circuited. The phase A lower IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.
37	<i>IGBT BU desat</i>	Trip	The <i>IGBT BU desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase B upper IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase B upper IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase B lower IGBT is short-circuited. The phase B upper IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.
38	<i>IGBT BL desat</i>	Trip	The <i>IGBT BL desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase B lower IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase B lower IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase B upper IGBT is short-circuited. The phase B lower IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
39	<i>IGBT CU desat</i>	Trip	The <i>IGBT CU desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase C upper IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase C upper IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase B lower IGBT is short-circuited. The phase B upper IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.
40	<i>IGBT CL desat</i>	Trip	The <i>IGBT CL desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the phase C lower IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the phase C lower IGBT is supporting large fault currents and that a serious bridge problem exists. Primary causes: The phase B upper IGBT is short-circuited. The phase B lower IGBT is defective. Possible board failures: DAMA BPIA BICL Possible wiring faults: The connections between BPIA and DAMA are missing or damaged.
41	<i>DC bus over voltage</i>	Trip	The <i>DC bus over voltage</i> trip fault occurs when the dc link voltage feedback (variable <i>DC bus voltage</i>) is too large. The over voltage threshold level is a function of the nominal dc link voltage, a function of the output line-line voltage (parameter <i>Max lineup output</i>). When the overvoltage condition is detected the gating to the bridge IGBTs is immediately disabled. The main purpose of the trip fault is to detect an excessive, potentially dangerous dc link voltage, and to respond by shutting down the bridge. Possible configuration faults: The parameter <i>Max lineup output</i>, power bridge output rated line-line voltage, is not set correctly. Possible board failures: BPIA/BPIB DSPX

Fault Code Descriptions

No.	Name	Type	Description
42	<i>EE erase failed</i>	Alarm	The <i>EE erase failed</i> trip fault occurs when the preparation of memory for the next parameter save operation fails to happen satisfactorily. The next parameter save operation is expected to be invalid, and the integrity of future parameter save operations are in doubt. <i>EE erase failed</i> requires a hard reset to clear. Possible board failures: DSPX
43	<i>Illegal charge seq</i>	Trip	The <i>Illegal charge seq</i> trip fault occurs when the link charge task has been given an illegal command. This should be considered as a code bug, should it occur. It can occur due to improper sequencing of an ACL sequencer design that has not followed sequencer/task rules.
44	<i>Illegal synch seq</i>	Trip	The <i>Illegal synch seq</i> trip fault occurs when the line synchronization task has been given an illegal command. This should be considered as a code bug, should it occur. It can occur due to improper sequencing of an ACL sequencer design that has not followed sequencer/task rules.
45	<i>Illegal enable seq</i>	Trip	The <i>Illegal enable seq</i> trip fault occurs when the regulator enable task has been given an illegal command. This should be considered as a code bug, should it occur. It can occur due to improper sequencing of an ACL sequencer design that has not followed sequencer/task rules.
46	<i>Gnd flt, coarse</i>	Trip	The <i>Gnd flt, coarse</i> trip fault occurs when a large ground current is detected. The trip fault occurs when the magnitude of the sum of the three phase currents is too large. Possible board failures: SHCA BPIB/BPIA HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.
47	<i>Gnd flt, filtered</i>	Trip	The <i>Gnd flt, filtered</i> trip fault occurs when a large ground current is detected. The trip fault occurs when the discriminated ground current (variable <i>Ground current</i>) is greater than the ground current trip fault threshold (parameter <i>Gnd flt trip level</i>). Possible configuration faults: The value of the ground current trip fault threshold, represented by parameter <i>Gnd flt trip level</i>, is too low. Possible board failures: SHCA BPIB/BPIA DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.

Fault Code Descriptions

No.	Name	Type	Description
48	<i>Gnd flt alarm</i>	Alarm	The <i>Gnd flt alarm</i> occurs when a large ground current is detected. The fault occurs when the discriminated ground current (variable <i>Ground current</i>) is greater than the ground current alarm level (parameter <i>Gnd flt alm level</i>). The alarm clears when the discriminated ground current drops below the ground current alarm turn off level (parameter <i>Gnd flt alm clr lvl</i>). Possible configuration faults: The value of the ground current alarm level, represented by parameter <i>Gnd flt alm level</i>, is too low. Possible board failures: SHCA BPIB/BPIA DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.
50	<i>HtSink temp low, B</i>	Trip	The <i>HtSink temp low, B</i> trip fault occurs when the heatsink B temperature (variable <i>Heat sink temp, B</i>) is too low. The main purpose of the trip fault is to detect the absence of the heatsink B thermal sensor input. Primary causes: The heatsink B thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 3 and 4, is missing or damaged.
51	<i>HtSink A temp low</i>	Trip	The <i>HtSink A temp low</i> trip fault occurs when the phase A heatsink temperature (variable <i>Phase A HtSink temp</i>) is too low. The main purpose of the trip fault is to detect the absence of the phase A heatsink thermal sensor input. Primary causes: The phase A heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.
52	<i>HtSink B temp low</i>	Trip	The <i>HtSink B temp low</i> trip fault occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is too low. The main purpose of the trip fault is to detect the absence of the phase B heatsink thermal sensor input. Primary causes: The phase B heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 3 and 4, is missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
53	<i>HtSink C temp low</i>	Trip	The <i>HtSink C temp low</i> trip fault occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is too low. The main purpose of the trip fault is to detect the absence of the phase C heatsink thermal sensor input. Primary causes: The phase C heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 5 and 6, is missing or damaged.
54	<i>Ambient temp low</i>	Trip	The <i>Ambient temp low</i> trip fault occurs when the ambient temperature (variable <i>Ambient temp</i>) is too low. The main purpose of the trip fault is to detect the absence of the ambient thermal sensor input. Primary causes: The ambient thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.
55	<i>HtSink B miswired</i>	Trip	The <i>HtSink B miswired</i> trip fault occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is high enough to indicate the presence of a thermal sensor input, and the phase B thermal sensor input is expected to be absent. Primary causes: The phase B heatsink thermal sensor input is present. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is present or the connector is damaged.
56	<i>HtSink C miswired</i>	Trip	The <i>HtSink C miswired</i> trip fault occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is high enough to indicate the presence of a thermal sensor input, and the phase C thermal sensor input is expected to be absent. Primary causes: The phase C heatsink thermal sensor input is present. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 5 and 6 is present or the connector is damaged.

Fault Code Descriptions

No.	Name	Type	Description
57	<i>HtSink sensor bad</i>	Alarm	The <i>HtSink sensor bad</i> alarm occurs when the heatsink temperature (variable <i>Heat sink temp</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the heatsink thermal sensor input. Primary causes: The heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.
58	<i>HtSink sensor A bad</i>	Alarm	The <i>HtSink sensor A bad</i> alarm occurs when the heatsink A temperature (variable <i>Heat sink temp, A</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the heatsink A thermal sensor input. Primary causes: The heatsink A thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.
59	<i>HtSink sensor B bad</i>	Alarm	The <i>HtSink sensor B bad</i> alarm occurs when the heatsink B temperature (variable <i>Heat sink temp, B</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the heatsink B thermal sensor input. Primary causes: The heatsink B thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 3 and 4, is missing or damaged.
60	<i>HtSink A sensor bad</i>	Alarm	The <i>HtSink A sensor bad</i> alarm occurs when the phase A heatsink temperature (variable <i>Phase A HtSink temp</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the phase A heatsink thermal sensor input. Primary causes: The phase A heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
61	<i>HtSink B sensor bad</i>	Alarm	The <i>HtSink B sensor bad</i> alarm occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the phase B heatsink thermal sensor input. Primary causes: The phase B heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 3 and 4, is missing or damaged.
62	<i>HtSink C sensor bad</i>	Alarm	The <i>HtSink C sensor bad</i> alarm occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is too far below the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to detect the absence of the phase C heatsink thermal sensor input. Primary causes: The phase C heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 5 and 6, is missing or damaged.
63	<i>HtSink over temp</i>	Trip	The <i>HtSink over temp</i> trip fault occurs when the heatsink temperature (variable <i>Heat sink temp</i>) is too large. The main purpose of the trip fault is to use the heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.

Fault Code Descriptions

No.	Name	Type	Description
64	<i>HtSink over temp, A</i>	Trip	The <i>HtSink over temp, A</i> trip fault occurs when the heatsink A temperature (variable <i>Heat sink temp, A</i>) is too large. The main purpose of the trip fault is to use the heatsink A temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink A temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.
65	<i>HtSink over temp, B</i>	Trip	The <i>HtSink over temp, B</i> trip fault occurs when the heatsink B temperature (variable <i>Heat sink temp, B</i>) is too large. The main purpose of the trip fault is to use the heatsink B temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink B temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged.
66	<i>HtSink A over temp</i>	Trip	The <i>HtSink A over temp</i> trip fault occurs when the phase A heatsink temperature (variable <i>Phase A HtSink temp</i>) is too large. The main purpose of the trip fault is to use the phase A heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.

Fault Code Descriptions

No.	Name	Type	Description
67	<i>HtSink B over temp</i>	Trip	The <i>HtSink B over temp</i> trip fault occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is too large. The main purpose of the trip fault is to use the phase B heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged.
68	<i>HtSink C over temp</i>	Trip	The <i>HtSink C over temp</i> trip fault occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is too large. The main purpose of the trip fault is to use the phase C heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 5 and 6 is damaged.
69	<i>HtSink temp hot</i>	Alarm	The <i>HtSink temp hot</i> alarm occurs when the heatsink temperature (variable <i>Heat sink temp</i>) is too large. The main purpose of the alarm is to use the heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.

Fault Code Descriptions

No.	Name	Type	Description
70	<i>HtSink temp hot, A</i>	Alarm	The <i>HtSink temp hot, A</i> alarm occurs when the heatsink A temperature (variable <i>Heat sink temp, A</i>) is too large. The main purpose of the alarm is to use the heatsink A temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink A temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.
71	<i>Htsink temp hot, B</i>	Alarm	The <i>Htsink temp hot, B</i> alarm occurs when the heatsink B temperature (variable <i>Heat sink temp, B</i>) is too large. The main purpose of the alarm is to use the heatsink B temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink B temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged.
72	<i>HtSink A temp hot</i>	Alarm	The <i>HtSink A temp hot</i> alarm occurs when the phase A heatsink temperature (variable <i>Phase A HtSink temp</i>) is too large. The main purpose of the alarm is to use the phase A heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged.

Fault Code Descriptions

No.	Name	Type	Description
73	<i>HtSink B temp hot</i>	Alarm	The <i>HtSink B temp hot</i> alarm occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is too large. The main purpose of the alarm is to use the phase B heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged.
74	<i>HtSink C temp hot</i>	Alarm	The <i>HtSink C temp hot</i> alarm occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is too large. The main purpose of the alarm is to use the phase C heatsink temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 5 and 6 is damaged.
75	<i>HtSink rise high</i>	Alarm	The <i>HtSink rise high</i> alarm occurs when the heatsink temperature (variable <i>Heat sink temp</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the heatsink and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
76	<i>HtSink rise high, A</i>	Alarm	The <i>HtSink rise high, A</i> alarm occurs when the heatsink A temperature (variable <i>Heat sink temp, A</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the heatsink A and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink A temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.
77	<i>HtSink rise high, B</i>	Alarm	The <i>HtSink rise high, B</i> alarm occurs when the heatsink B temperature (variable <i>Heat sink temp, B</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the heatsink B and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the heatsink B temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.
78	<i>HtSink A rise high</i>	Alarm	The <i>HtSink A rise high</i> alarm occurs when the phase A heatsink temperature (variable <i>Phase A HtSink temp</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the phase A heatsink and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 1 and 2 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
79	<i>HtSink B rise high</i>	Alarm	The <i>HtSink B rise high</i> alarm occurs when the phase B heatsink temperature (variable <i>Phase B HtSink temp</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the phase B heatsink and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 3 and 4 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.
80	<i>HtSink C rise high</i>	Alarm	The <i>HtSink C rise high</i> alarm occurs when the phase C heatsink temperature (variable <i>Phase C HtSink temp</i>) is too far above the ambient temperature (variable <i>Ambient temp</i>). The main purpose of the alarm is to use the phase C heatsink and ambient temperature measurements to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C heatsink temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 5 and 6 is damaged. The thermal sensor, input to backplane connector J4 pins 7 and 8, is missing or damaged.
81	<i>HtSink temp imbalanc</i>	Alarm	The <i>HtSink temp imbalanc</i> alarm occurs when the difference between two of the heatsink temperatures differ is too large. In the 250, 375, and 620 frame sizes the heatsink temperatures are contained in variables <i>Heat sink temp, A</i> and <i>Heat sink temp, B</i>. In the 1000 and 1800 frame sizes the heatsink temperatures are contained in variables <i>Phase A HtSink temp</i>, <i>Phase B HtSink temp</i>, and <i>Phase C HtSink temp</i>. Primary causes: The bridge environment and running conditions cause the heatsink temperatures to differ by a large amount. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged. The thermal sensor, input to backplane connector J4 pins 3 and 4, is missing or damaged. The thermal sensor, input to backplane connector J4 pins 5 and 6, is missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
82	<i>HtSink conf invalid</i>	Trip	The <i>HtSink conf invalid</i> trip fault occurs when the specified power bridge heatsink configuration is invalid.
83	<i>HtSink temp low</i>	Trip	The <i>HtSink temp low</i> trip fault occurs when the heatsink temperature (variable <i>Heat sink temp</i>) is too low. The main purpose of the trip fault is to detect the absence of the heatsink thermal sensor input. Primary causes: The heatsink thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.
84	<i>HtSink temp low, A</i>	Trip	The <i>HtSink temp low, A</i> trip fault occurs when the heatsink A temperature (variable <i>Heat sink temp, A</i>) is too low. The main purpose of the trip fault is to detect the absence of the heatsink A thermal sensor input. Primary causes: The heatsink A thermal sensor input is not present. Possible board failures: BICL Possible wiring faults: The thermal sensor, input to backplane connector J4 pins 1 and 2, is missing or damaged.
86	<i>AC line over voltage</i>	Trip	The <i>ac line over voltage</i> trip fault occurs when the control firmware detects that the magnitude of the ac line is above the value of <i>Line OV fault lvl</i>, which has a suggested value of 117% of nominal. The voltage magnitude used for this comparison is a processed by a low-pass filter. This filter is set to 1.2 rad/sec as a default, so transient over-voltages are allowed above the threshold value without causing this trip fault. Primary causes: AC line voltage is excessive. Possible configuration faults: Source has been applied at a voltage other than that set by the factory. Factory setting is <i>ac input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BP1A/BP1B BICL DSPX

Fault Code Descriptions

No.	Name	Type	Description
87	AC line voltage high	Alarm	The <i>ac line voltage high</i> alarm occurs when the control firmware detects that the magnitude of the ac line is above the value of <i>Line OV alm on lvl</i>, which has a suggested value of 112% of nominal. The voltage magnitude used for this comparison is a low-pass filtered version of the fastest version. The filter is set to 1.2 rad/sec as a default, so transient voltage above the alarm turn-on value can occur without causing this alarm. This alarm will cease once the filtered value of voltage magnitude has decreased to below <i>Line OV alm off lvl</i>, which has a suggested value of 110% of nominal. Primary causes: AC line voltage is marginally excessive. Possible configuration faults: Source has been applied at a voltage other than that set by the factory. Factory setting is <i>ac input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BP1A/BP1B B1CL DSPX
88	AC line under volt	Trip	The <i>ac line under volt</i> trip fault occurs when the control firmware detects that the magnitude of the ac line is below the value of <i>Line UV fault lvl</i>, which has a suggested value of 50% of the nominal ac line input. The voltage magnitude used for this comparison is a low-pass filtered version of the signal. The filter is set to 1.2 rad/sec as a default, so transient voltages below the alarm turn-on value can occur without causing this trip fault. Primary causes: AC line voltage too low. Possible configuration faults: Source has been applied at a voltage other than that set by the factory. Factory setting is <i>ac input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BP1A/BP1B B1CL DSPX

Fault Code Descriptions

No.	Name	Type	Description
89	AC line volts low	Alarm	The ac <i>line volts low</i> alarm occurs when the control firmware detects that the magnitude of the ac line is below the value of <i>Line UV alm on lvl</i>, which has a suggested value of 88% of nominal. The voltage magnitude used for this comparison is a low-pass filtered version of the fastest version. The filter is set to 1.2 rad/sec as a default, so transient voltage above the alarm turn-on value can occur without causing this alarm. This alarm will cease once the filtered value of voltage magnitude has increased to above the value of <i>Line UV alm off lvl</i>, which has a suggested value of 90% of nominal. Primary causes: AC line voltage is marginally low. Possible configuration faults: Source has been applied at a voltage other than that set by the factory. Factory setting is ac <i>input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BPIA/BPIB BICL DSPX
90	AC line over freq	Trip	The ac <i>line over freq</i> trip fault occurs when the control firmware detects that the frequency of the ac line is above the value of <i>Over frq flt lvl</i>, which has a suggested value of 125% of nominal. The frequency value used for this comparison is a low-pass filtered version of the fastest version. The filter is set to .2 rad/sec as a default, so transient over-frequency values are allowed above the threshold value without causing this trip fault. Primary causes: AC line frequency is excessive. Possible configuration faults: Source has been applied at a 60hz while the factory setup value, <i>Input frequency</i> was at 50hz. Factory setting is ac <i>input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BPIA/BPIB BICL DSPX

Fault Code Descriptions

No.	Name	Type	Description
91	<i>AC line freq high</i>	Alarm	The <i>ac line freq high</i> alarm occurs when the control firmware detects that the frequency of the ac line is above the value of <i>Over frq alm on lvl</i>, which has a suggested value of nominal frequency plus 17.3 rad/sec. The frequency value used for this comparison is a low-pass filtered version of the fastest version. The filter is set to .2 rad/sec as a default, so transient over-frequency values are allowed above the threshold value without causing this alarm. This alarm will cease once the filtered value of the filtered frequency has decreased to below the value of <i>Over frq alm off lvl</i>, which has a suggested value of nominal frequency plus 15.7rad/sec. Primary causes: AC line frequency is marginally excessive. Possible configuration faults: Source has been applied 60hz, while the factory setup value, <i>Input frequency</i>, was at 50hz. Factory setting is <i>ac input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BPIA/BPIB BICL DSPX
92	<i>AC line under freq</i>	Trip	The <i>ac line under freq</i> trip fault occurs when the control firmware detects that the frequency of the ac line is below the value of <i>Low frq flt lvl</i>, which has a suggested value of nominal of 50% of nominal. The frequency value used for this comparison is a low-pass filtered version of the fastest version. The filter is set to .2 rad/sec as a default; therefore, transient under-frequency values are allowed below the threshold value without causing this trip fault. Primary causes: AC line frequency is low. Possible configuration faults: Source has been applied at 50hz, while the factory setup value, <i>Input frequency</i>, was at 60hz. Factory setting is <i>ac input voltage</i>. Care must be taken when changing this parameter, as the bridge may not be rated for that voltage. Possible board failures: BPIA/BPIB BICL DSPX

Fault Code Descriptions

No.	Name	Type	Description
93	<i>AC line freq low</i>	Alarm	The <i>ac line freq low</i> alarm occurs when the control firmware detects that the frequency of the ac line is below the value of <i>Low frq alm on lvl</i>, which has a suggested value of nominal minus 17.3rad/sec. The frequency value used for this comparison is a low-pass filtered version of the fastest version. The filter is set to .2 rad/sec as a default; therefore, transient under-frequency values are allowed below the threshold value without causing this alarm. This alarm will cease once the filtered value of the filtered frequency has increased to a value above or below the value of <i>Low frq alm off lvl</i>, which has a suggested value of nominal frequency minus 15.7rad/sec. Primary causes: AC line frequency is transiently low. Possible configuration faults: Source has been applied at 50hz, while the factory setup value, <i>Input frequency</i> was at 60hz. Possible board failures: BP1A/BP1B BICL DSPX
94	<i>IGBT AU over temp</i>	Trip	The <i>IGBT AU over temp</i> trip fault occurs when the phase A upper IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase A upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A upper IGBT junction temperature to rise above a safe operating level.
95	<i>IGBT BU over temp</i>	Trip	The <i>IGBT BU over temp</i> trip fault occurs when the phase B upper IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase B upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B upper IGBT junction temperature to rise above a safe operating level.
96	<i>IGBT CU over temp</i>	Trip	The <i>IGBT CU over temp</i> trip fault occurs when the phase C upper IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase C upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C upper IGBT junction temperature to rise above a safe operating level.
97	<i>IGBT AL over temp</i>	Trip	The <i>IGBT AL over temp</i> trip fault occurs when the phase A lower IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase A lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A lower IGBT junction temperature to rise above a safe operating level.

Fault Code Descriptions

No.	Name	Type	Description
98	<i>IGBT BL over temp</i>	Trip	The <i>IGBT BL over temp</i> trip fault occurs when the phase B lower IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase B lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B lower IGBT junction temperature to rise above a safe operating level.
99	<i>IGBT CL over temp</i>	Trip	The <i>IGBT CL over temp</i> trip fault occurs when the phase C lower IGBT junction temperature is too large. The main purpose of the trip fault is to use the phase C lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C lower IGBT junction temperature to rise above a safe operating level.
100	<i>IGBT AU temp hot</i>	Alarm	The <i>IGBT AU temp hot</i> alarm occurs when the phase A upper IGBT junction temperature is too large. The main purpose of the alarm is to use the phase A upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A upper IGBT junction temperature to rise above a safe operating level.
101	<i>IGBT BU temp hot</i>	Alarm	The <i>IGBT BU temp hot</i> alarm occurs when the phase B upper IGBT junction temperature is too large. The main purpose of the alarm is to use the phase B upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B upper IGBT junction temperature to rise above a safe operating level.
102	<i>IGBT CU temp hot</i>	Alarm	The <i>IGBT CU temp hot</i> alarm occurs when the phase C upper IGBT junction temperature is too large. The main purpose of the alarm is to use the phase C upper IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C upper IGBT junction temperature to rise above a safe operating level.
103	<i>IGBT AL temp hot</i>	Alarm	The <i>IGBT AL temp hot</i> alarm occurs when the phase A lower IGBT junction temperature is too large. The main purpose of the alarm is to use the phase A lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase A lower IGBT junction temperature to rise above a safe operating level.

Fault Code Descriptions

No.	Name	Type	Description
104	<i>IGBT BL temp hot</i>	Alarm	The <i>IGBT BL temp hot</i> alarm occurs when the phase B lower IGBT junction temperature is too large. The main purpose of the alarm is to use the phase B lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase B lower IGBT junction temperature to rise above a safe operating level.
105	<i>IGBT CL temp hot</i>	Alarm	The <i>IGBT CL temp hot</i> alarm occurs when the phase C lower IGBT junction temperature is too large. The main purpose of the alarm is to use the phase C lower IGBT junction temperature calculated by the bridge thermal model to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the phase C lower IGBT junction temperature to rise above a safe operating level.
106	<i>Ambient over temp</i>	Trip	The <i>Ambient over temp</i> trip fault occurs when the ambient temperature (variable <i>Ambient temp</i>) is too high. The main purpose of the trip fault is to use the ambient temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the ambient temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 7 and 8 is damaged.
107	<i>Ambient temp hot</i>	Alarm	The <i>Ambient temp hot</i> alarm occurs when the ambient temperature (variable <i>Ambient temp</i>) is too high. The main purpose of the alarm is to use the ambient temperature measurement to detect a condition that could endanger the power bridge. Primary causes: The bridge environment and running conditions cause the ambient temperature to rise above a safe operating level. Possible board failures: BICL Possible wiring faults: The thermal sensor input to backplane connector J4 pins 7 and 8 is damaged.

Fault Code Descriptions

No.	Name	Type	Description
108	<i>Reg in lim time out</i>	Trip	The <i>Reg in lim time out</i> trip fault occurs when any one or more of several regulator outputs is restricted by a clamp for one second. The variable <i>Reg limit summary</i> stores the summary of all regulator limit bits the last time any regulator was in limit. This is a good way to see what limit caused the trip fault. A list of the bit numbers for specific regulator limit flags that are part of <i>Reg limit summary</i> given below. Phase lock loop regulator: Maximum frequency limit -- bit 0 Minimum frequency limit -- bit 1 Voltage regulator: X-axis current command output in maximum limit -- bit 2 X-axis current command output in minimum limit -- bit 3 Current regulator: Bits 8 and 10 set or only bit 10 if spillover disabled -- bit 4 Bits 9 and 11 set or only bit 11 if spillover disabled -- bit 5 Y-channel up/down command in maximum limit -- bit 6 Y-channel up/down command in minimum limit -- bit 7 Y-channel current command in maximum limit -- bit 8 Y-channel current command in minimum limit -- bit 9 X-channel up/down command in maximum limit -- bit 10 X-channel up/down command in minimum limit -- bit 11 If a particular limit is suspected, it may be checked by viewing the associated indication variable, as listed in the table below. Note that a very helpful diagram can be found at Diagrams/Contents/Ovr_Reg_Lim. Variable Description <i>PLL positive limit</i> The pll is in the maximum limit <i>PLL lower limit</i> The pll is in the minimum limit <i>Ireg X pos limit</i> The x-channel current command from the voltage regulator is in limit positive limit. <i>Ireg X neg limit</i> The x-channel current command from the voltage regulator is in negative limit. <i>Ix U/D in pos lim</i> The x-channel output of the inner current regulator is in limit positive limit. If the spillover gain is non-zero, this flag will not cause an alarm or fault even though it is active. This is always the case because of the controls calculation. <i>Ix U/D in neg lim</i> The x-channel output of the inner current regulator is in negative limit. When the spillover gain is non-zero, this flag will not cause an alarm or fault even though it is active. This is always the case because of the controls calculation. <i>Ireg Y U/D pos limit</i> This flag is set when the y-axis current regulator modulation command is in its positive limit.

Fault Code Descriptions

No.	Name	Type	Description
109	<i>Ckt board list fail</i>	Trip	The <i>Ckt board list fail</i> trip fault occurs when the electronic board ID interrogation, which happens during drive initialization, fails. Each circuit board in the rack has an electronic ID. <i>Ckt board list fail</i> requires a hard reset to clear. Primary causes: A circuit board is not seated properly in its backplane sockets. The electronic ID part on a circuit board has experienced a failure.
110	<i>Task 1 exec overrun</i>	Alarm	The <i>Task 1 exec overrun</i> alarm occurs when Task 1 exceeds its allotted CPU execution time. This alarm may occur during system development but should not occur in the field. Primary causes: Task 1 contains too much functionality to complete in the specified execution time. Possible board failures: DSPX
111	<i>Task 2 exec overrun</i>	Alarm	The <i>Task 2 exec overrun</i> alarm occurs when Task 2 exceeds its allotted CPU execution time. This alarm may occur during system development but should not occur in the field. Primary causes: Task 2 contains too much functionality to complete in the specified execution time. Task 1 contains too much functionality. Although it completes in its specified execution time, it does not allow Task 2 to run to completion. Possible board failures: DSPX
112	<i>Task 3 exec overrun</i>	Alarm	The <i>Task 3 exec overrun</i> alarm occurs when Task 3 exceeds its allotted CPU execution time. This alarm may occur during system development but should not occur in the field. Primary causes: Task 3 contains too much functionality to complete in the specified execution time. Task 1 and Task 2 contain too much functionality. Although they complete in their specified execution time, they do not allow Task 3 to run to completion. Possible board failures: DSPX

Fault Code Descriptions

No.	Name	Type	Description
113	<i>Invalid board set</i>	Trip	The <i>Invalid board set</i> trip fault occurs when the electronic board ID interrogation, which happens during initialization, does not produce the expected set of circuit boards. Each circuit board in the rack has an electronic ID that contains board type and revision information. Each Innovation Series product has an expected set of circuit boards. If any of the expected boards is missing, or if incorrect boards are present, the drive cannot operate properly. The circuit boards that the drive has identified can be obtained by making the following toolbox menu selections: View, Reports, Drive Version and Hardware Info. Primary causes: A circuit board that is required for the drive to operate properly is not present. A circuit board that should not be used in the drive is present. A circuit board is not seated properly in its backplane socket. The electronic ID part on a circuit board has experienced a failure.
114	<i>Ain 1 signal alarm</i>	Alarm	The <i>Ain 1 signal alarm</i> occurs when the level of analog input number 1 (variable <i>Analog input 1</i>) is too low. The alarm level is specified by parameter <i>Analog in 1 flt lev</i>. The alarm can occur only when parameter <i>Analog in 1 flt mode</i> is set equal to Low level alarm. The alarm is disabled for any other setting for parameter <i>Analog in 1 flt mode</i>. The main purpose of <i>Ain 1 signal alarm</i> is to detect a low 4-20 mA signal. The low level may indicate that a signal is missing which is required for the drive to operate properly. Primary causes: The analog input number 1 signal source is absent or unhealthy. Possible configuration faults: The analog input 1 alarm level, represented by parameter <i>Analog in 1 flt lev</i>, is set incorrectly. The analog input number 1 gain, represented by parameter <i>Analog in 1 gain</i>, is set incorrectly. The analog input number 1 offset, represented by parameter <i>Analog in 1 offset</i>, is set incorrectly. The analog input number in 1 flt mode, represented by parameter <i>Analog in 1 flt mode</i>, is set incorrectly. Possible wiring faults: The connections between the analog signal source and ATBA terminal board locations 38 (AI1P) and 40 (AI1N) are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
115	<i>Ain 1 signal trip</i>	Trip	The <i>Ain 1 signal trip</i> fault occurs when the level of analog input number 1 (variable <i>Analog input 1</i>) is too low. The trip fault level is specified by parameter <i>Analog in 1 flt lev</i>. The trip fault can occur only when parameter <i>Analog in 1 flt mode</i> is set equal to Low level trip. The trip fault is disabled for any other setting for parameter <i>Analog in 1 flt mode</i>. The main purpose of <i>Ain 1 signal trip</i> is to detect a low 4-20 mA signal. The low level may indicate that a signal is missing which is required for the drive to operate properly. Primary causes: The analog input number 1 signal source is absent or unhealthy. Possible configuration faults: The analog input 1 trip fault level, represented by parameter <i>Analog in 1 flt lev</i>, is set incorrectly. The analog input number 1 gain, represented by parameter <i>Analog in 1 gain</i>, is set incorrectly. The analog input number 1 offset, represented by parameter <i>Analog in 1 offset</i>, is set incorrectly. The analog input number in 1 flt mode, represented by parameter <i>Analog in 1 flt mode</i>, is set incorrectly. Possible wiring faults: The connections between the analog signal source and ATBA terminal board locations 38 (AI1P) and 40 (AI1N) are missing or damaged.
116	<i>Ain 2 signal alarm</i>	Alarm	The <i>Ain 2 signal alarm</i> occurs when the level of analog input number 2 (variable <i>Analog input 2</i>) is too low. The alarm level is specified by parameter <i>Analog in 2 flt lev</i>. The alarm can occur only when parameter <i>Analog in 2 flt mode</i> is set equal to Low level alarm. The fault is disabled for any other setting for parameter <i>Analog in 2 flt mode</i>. The main purpose of <i>Ain 2 signal alarm</i> is to detect a low 4-20 mA signal. The low level may indicate that a signal is missing which is required for the drive to operate properly. Primary causes: The analog input number 2 signal source is absent or unhealthy. Possible configuration faults: The analog input 2 alarm level, represented by parameter <i>Analog in 2 flt lev</i>, is set incorrectly. The analog input number 2 gain, represented by parameter <i>Analog in 2 gain</i>, is set incorrectly. The analog input number 2 offset, represented by parameter <i>Analog in 2 offset</i>, is set incorrectly. The analog input number in 2 flt mode, represented by parameter <i>Analog in 2 flt mode</i>, is set incorrectly. Possible wiring faults: The connections between the analog signal source and ATBA terminal board locations 44 (AI2P) and 46 (AI2N) are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
117	<i>Ain 2 signal trip</i>	Trip	The <i>Ain 2 signal trip</i> fault occurs when the level of analog input number 2 (variable <i>Analog input 2</i>) is too low. The trip fault level is specified by parameter <i>Analog in 2 flt lev</i>. The trip fault can occur only when parameter <i>Analog in 2 flt mode</i> is set equal to Low level trip. The trip fault is disabled for any other setting for parameter <i>Analog in 2 flt mode</i>. The main purpose of <i>Ain 2 signal trip</i> is to detect a low 4-20 mA signal. The low level may indicate that a signal is missing which is required for the drive to operate properly. Primary causes: The analog input number 2 signal source is absent or unhealthy. Possible configuration faults: The analog input 2 trip fault level, represented by parameter <i>Analog in 2 flt lev</i>, is set incorrectly. The analog input number 2 gain, represented by parameter <i>Analog in 2 gain</i>, is set incorrectly. The analog input number 2 offset, represented by parameter <i>Analog in 2 offset</i>, is set incorrectly. The analog input number in 2 flt mode, represented by parameter <i>Analog in 2 flt mode</i>, is set incorrectly. Possible wiring faults: The connections between the analog signal source and ATBA terminal board locations 44 (AI2P) and 46 (AI2N) are missing or damaged.
118	<i>IGBT AU bridg1 desat</i>	Trip	The <i>IGBT AU bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase A upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase A upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase A lower IGBT is short circuited. The bridge 1 phase A upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
119	<i>IGBT AL bridg1 desat</i>	Trip	The <i>IGBT AL bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase A lower IGBT to turn on and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase A lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase A upper IGBT is short circuited. The bridge 1 phase A lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
120	<i>IGBT BU bridg1 desat</i>	Trip	The <i>IGBT BU bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase B upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase B upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase B lower IGBT is short circuited. The bridge 1 phase B upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
121	<i>IGBT BL bridg1 desat</i>	Trip	The <i>IGBT BL bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase B lower IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase B lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase B upper IGBT is short circuited. The bridge 1 phase B lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
122	<i>IGBT CU bridg1 desat</i>	Trip	The <i>IGBT CU bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase C upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase C upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase C lower IGBT is short circuited. The bridge 1 phase C upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
123	<i>IGBT CL bridg1 desat</i>	Trip	The <i>IGBT CL bridg1 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 1 phase C lower IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 1 phase C lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 1 phase C upper IGBT is short circuited. The bridge 1 phase C lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
124	<i>IGBT AU bridg2 desat</i>	Trip	The <i>IGBT AU bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase A upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase A upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase A lower IGBT is short circuited. The bridge 2 phase A upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
125	<i>IGBT AL bridg2 desat</i>	Trip	The <i>IGBT AL bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase A lower IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase A lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase A upper IGBT is short circuited. The bridge 2 phase A lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
126	<i>IGBT BU bridg2 desat</i>	Trip	The <i>IGBT BU bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase B upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase B upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase B lower IGBT is short circuited. The bridge 2 phase B upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
127	<i>IGBT BL bridg2 desat</i>	Trip	The <i>IGBT BL bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase B lower IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase B lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase B upper IGBT is short circuited. The bridge 2 phase B lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
128	<i>IGBT CU bridg2 desat</i>	Trip	The <i>IGBT CU bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase C upper IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase C upper IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase C lower IGBT is short circuited. The bridge 2 phase C upper IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.
129	<i>IGBT CL bridg2 desat</i>	Trip	The <i>IGBT CL bridg2 desat</i> trip fault is hardware generated. The trip fault occurs when the bridge control commands the bridge 2 phase C lower IGBT to turn on, and the measured collector-emitter voltage of the IGBT is greater than 10 V. Under normal conditions when the IGBT is turned on a voltage of 3 V to 5 V develops across the collector-emitter junction. Voltages greater than 10 V across the junction suggest that the bridge 2 phase C lower IGBT is supporting large fault currents, and that a serious bridge problem exists. Primary causes: The bridge 2 phase C upper IGBT is short circuited. The bridge 2 phase C lower IGBT is defective. Possible board failures: DAMA BPIB BICL Possible wiring faults: The connections between BPIB and DAMA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
130	<i>Current imbal phs A</i>	Trip	The <i>Current imbal phs A</i> trip fault is hardware generated. The trip fault occurs when the difference between the bridge 1 and bridge 2 phase A shunt currents over a time interval is too large. A 10 percent imbalance over an 88 microsecond measurement period qualifies as a fault condition. A bridge 1 to bridge 2 shoot through in phase A causes a fault in about 8 microseconds. When the imbalance condition is detected, the power bridge IGBT gating is disabled immediately. Primary causes: A short circuit exists across or through one or more of the phase A IGBTs. One of the phase A shunts is reversed. Possible board failures: SHCA BPIB BICL Possible wiring faults: The connections between BPIB and SHCA are missing or damaged.
131	<i>Current imbal phs B</i>	Trip	The <i>Current imbal phs B</i> trip fault is hardware generated. The trip fault occurs when the difference between the bridge 1 and bridge 2 phase B shunt currents over a time interval is too large. A 10 percent imbalance over an 88 microsecond measurement period qualifies as a fault condition. A bridge 1 to bridge 2 shoot through in phase B causes a fault in about 8 microseconds. When the imbalance condition is detected, the power bridge IGBT gating is disabled immediately. Primary causes: A short circuit exists across or through one or more of the phase B IGBTs. One of the phase B shunts is reversed. Possible board failures: SHCA BPIB BICL Possible wiring faults: The connections between BPIB and SHCA are missing or damaged.
132	<i>Current imbal phs C</i>	Trip	The <i>Current imbal phs C</i> trip fault is hardware generated. The trip fault occurs when the difference between the bridge 1 and bridge 2 phase C shunt currents over a time interval is too large. A 10 percent imbalance over an 88 microsecond measurement period qualifies as a fault condition. A bridge 1 to bridge 2 shoot through in phase C causes a fault in about 8 microseconds. When the imbalance condition is detected, the power bridge IGBT gating is disabled immediately. Primary causes: A short circuit exists across or through one or more of the phase C IGBTs. One of the phase C shunts is reversed. Possible board failures: SHCA BPIB BICL Possible wiring faults: The connections between BPIB and SHCA are missing or damaged.

Fault Code Descriptions

No.	Name	Type	Description
133	<i>Xfrmr over temp</i>	Trip	The <i>Xfrmr over temp</i> trip occurs when the transformer over temperature circuit is open. The control input pointing to the over temperature circuit is selected by parameter <i>Xfrmr OT fault sel</i> . <i>Xfrmr over temp</i> can be disabled by setting parameter <i>Xfrmr OT fault sel</i> equal to <i>Unused</i> .
134	<i>Xfrmr temp hot</i>	Alarm	The <i>Xfrmr temp hot</i> alarm occurs when the transformer over temperature circuit is open. The control input pointing to the over temperature circuit is selected by parameter <i>Xfrmr OT fault sel</i> . <i>Xfrmr temp hot</i> can be disabled by setting parameter <i>Xfrmr OT fault sel</i> equal to <i>Unused</i> .
137	<i>Unrecognized IPN</i>	Trip	The <i>Unrecognized IPN</i> trip fault occurs when the specified Intelligent Part Number (IPN) is not a valid combination of fields for the Innovation Series product. The IPN should correspond to the drive nameplate. <i>Unrecognized IPN</i> requires a hard reset to clear.
139	<i>Customer use NC flt</i>	Trip	The <i>Customer use NC flt</i> trip fault occurs when the customer normally closed circuit is open. The state of the normally closed circuit is selected by parameter <i>User NC fault sel</i> .
140	<i>Customer use NC alm</i>	Alarm	The <i>Customer use NC alm</i> alarm occurs when the customer normally closed circuit is open. The state of the normally closed circuit is selected by parameter <i>User NC fault sel</i> .
141	<i>Customer use NO flt</i>	Trip	The <i>Customer use NO flt</i> trip fault occurs when the customer normally open circuit is closed. The state of the normally open circuit is selected by parameter <i>User NO fault sel</i> .
142	<i>Customer use NO alm</i>	Alarm	The <i>Customer use NO alm</i> alarm occurs when the customer normally open circuit is closed. The state of the normally open circuit is selected by parameter <i>User NO fault sel</i> .
145	<i>A-B voltage offset</i>	Trip	The <i>A-B voltage offset</i> trip fault occurs when the A-B line-line voltage offset (variable <i>A-B, Voltage offset</i>) is too large. <i>A-B voltage offset</i> evaluates A-B voltage feedback information collected while the power bridge is turned on. It uses the information to continuously adjust the voltage offset, and to detect power bridge and feedback circuitry problems. Primary causes: The wire connection between the phase A or phase B SHCA card, and the BPIA/BPIB card is missing or damaged. The A-B voltage feedback VCO on the BPIA/BPIB card is damaged. Two or more shorted IGBTs in separate phases of the power bridge exist. A combination of a shorted IGBT in phase A or phase B, and a ground in the load exists. Possible board failures: SHCA BPIA/BPIB HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.

Fault Code Descriptions

No.	Name	Type	Description
146	<i>B-C voltage offset</i>	Trip	The <i>B-C voltage offset</i> trip fault occurs when the B-C line-line voltage offset (variable <i>B-C, Voltage offset</i>) is too large. <i>B-C voltage offset</i> evaluates B-C voltage feedback information collected while the power bridge is turned on. It uses the information to continuously adjust the voltage offset, and to detect power bridge and feedback circuitry problems. Primary causes: The wire connection between the phase B or phase C SHCA card, and the BPIA/BPIB card is missing or damaged. The B-C voltage feedback VCO on the BPIA/BPIB card is damaged. Two or more shorted IGBTs in separate phases of the power bridge exist. A combination of a shorted IGBT in phase A or phase B, and a ground in the load exists. Possible board failures: SHCA BPIA/BPIB HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.
147	<i>Phase A cur offset</i>	Trip	The <i>Phase A cur offset</i> trip fault occurs when the phase A current offset (variable <i>Phs A current offset</i>) is too large. The current offset threshold level is 1 percent of the rated shunt current. <i>Phs A current offset</i> is the output of an automatic current offset calculation. <i>Phase A cur offset</i> evaluates phase A current feedback information collected while the power bridge is turned off, when current feedbacks should be zero. It uses the information to detect power bridge and feedback circuitry problems. Primary causes: The wire connection between the phase A SHCA card and the BPIA/BPIB card is missing or damaged. The phase A current feedback VCO on the BPIA/BPIB card is damaged. Two or more shorted IGBTs in the power bridge exist. A combination of a shorted IGBT in the power bridge and a ground in the load exists. Possible configuration faults: The specified frame size, represented by parameter <i>IPN frame size</i>, does not match the bridge. Possible board failures: SHCA BPIA/BPIB HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.

Fault Code Descriptions

No.	Name	Type	Description
148	<i>Bic Watchdog</i>	Trip	The <i>Bic Watchdog</i> trip fault occurs when the BICL stops seeing a watchdog toggle bit from the DSPX. When the drive is running, BICL monitors a toggle bit being manipulated by DSPX. If DSPX does not toggle the bit on BICL within a predefined time interval, the BICL declares a fault, and disables the bridge. This indicates that the processor cannot communicate reliably with the bridge interface card. <i>Bic Watchdog</i> requires a hard reset to clear. Possible configuration faults: The connected drive is a simulator but <i>Simulate mode act</i> is equal to <i>False</i>. Set <i>Simulate mode</i> equal to <i>Yes</i> to correct the problem. Possible board failures: BICL DSPX CABP (backplane)
149	<i>DSPx Watchdog</i>	Trip	The <i>DSPx Watchdog</i> trip fault occurs when the DSPX EPLD stops seeing a watchdog toggle bit from the processor. A hard reset occurs, and the fault is declared at initialization. <i>DSPx Watchdog</i> requires a hard reset to clear. Possible board failures: DSPX
151	<i>Phase C cur offset</i>	Trip	The <i>Phase C cur offset</i> trip fault occurs when the phase C current offset (variable <i>Phs C current offset</i>) is too large. The current offset threshold level is 1 percent of the rated shunt current. <i>Phs C current offset</i> is the output of an automatic current offset calculation. <i>Phase C cur offset</i> evaluates phase C current feedback information collected while the power bridge is turned off, when current feedbacks should be zero. It uses the information to detect power bridge and feedback circuitry problems. Primary causes: The wire connection between the phase C SHCA card, and the BPIA/BPIB card is missing or damaged. The phase C current feedback VCO on the BPIA/BPIB card is damaged. Two or more shorted IGBTs in the power bridge exist. A combination of a shorted IGBT in the power bridge, and a ground in the load exists. Possible configuration faults: The specified frame size, represented by parameter <i>IPN frame size</i>, does not match the bridge. Possible board failures: SHCA BPIA/BPIB HFPA (FU4) DSPX Possible wiring faults: Connection between BPIA/BPIB and SHCA.

Fault Code Descriptions

No.	Name	Type	Description
154	<i>Bic watchdog echo</i>	Trip	The <i>Bic watchdog echo</i> trip fault occurs when the DSPX stops seeing the echo of the watchdog toggle bit that it writes to the BICL. This indicates that the processor cannot communicate reliably with the bridge interface card. Primary Causes: Bent backplane connector pins or poorly seated cards. Possible board failures: BICL DSPX CABP (backplane)
156	<i>LAN trip request</i>	Trip	The <i>LAN trip request</i> trip fault occurs when a request for a trip fault is received from the LAN by assertion of the reference Boolean signal <i>Trip request, lan</i> .
157	<i>LAN alarm request</i>	Alarm	The <i>LAN alarm request</i> alarm occurs when a request for an alarm is received from the LAN by assertion of the reference Boolean signal <i>Alarm request, lan</i> .
158	<i>LAN watchdog alarm</i>	Alarm	The <i>LAN watchdog alarm</i> occurs when the connection between DSPX and the Application/LAN interface becomes invalid. This includes one of the following conditions, depending upon the selection of <i>Network interface</i>: The Application/LAN interface Dual-Port RAM watchdog stops. The ISBus frames stop. The alarm is declared after the condition persists for several hundred microseconds.
160	<i>LAN heartbeat trip</i>	Trip	The <i>LAN heartbeat trip</i> occurs when all of the following conditions are present: Non-zero value is entered in Parameter <i>LAN heartbeat time</i>. The signal (<i>Heartbeat ref, lan</i>) fails to transition within in that time. The trip behavior is enabled by Parameter <i>LAN trips inhibit</i>. The <i>LAN connection ok</i> condition was previously detected.
161	<i>LAN heartbeat alarm</i>	Alarm	The <i>LAN heartbeat alarm</i> occurs when all of the following conditions are present: Non-zero value is entered in Parameter <i>LAN heartbeat time</i>. The signal (<i>Heartbeat ref, lan</i>) fails to transition within in that time. Either the trip behavior is inhibited by Parameter <i>LAN trips inhibit</i>, or the trip behavior is enabled but the <i>LAN connection ok</i> condition was not previously detected.
162	<i>System ISBus error</i>	Alarm	The <i>System ISBus error</i> alarm occurs when an ISBus fault is detected in the DSPX control. The variable <i>Sys ISBus error reg</i> contains the bit-coded value of the last ISBus fault detected; each bit indicates a particular ISBus fault seen by the control. The variable <i>Sys ISBus error cnt</i> increments upon fault detection. Record the value of <i>Sys ISBus error reg</i> to assist factory troubleshooting efforts. Monitor the progression of <i>Sys ISBus error cnt</i> to obtain an indication of the rate of occurrence of fault conditions. Transient occurrence of this alarm upon initialization of the interface is expected.

Fault Code Descriptions

No.	Name	Type	Description
163	<i>Frame PLL not OK</i>	Alarm	The <i>Frame PLL not OK</i> alarm occurs when phase-lock between the DSPX control and the System ISBus or (local ACL) is not assured. Detection of the fault is enabled when the parameter <i>Network interface</i> is configured to select an interface for which synchronized operation is supported. The presence of this alarm indicates that data coherency is compromised. Verify the integrity of IsBus connections and configurations. If this alarm persists in the absence of any other interface faults, then verify that <i>LAN frame time</i> is consistent with that of the host, and confirm the absence of overrides, particularly regarding the Frame phaselock loop and DSPX timebase. Transient occurrence of this alarm upon initialization of the interface is expected.

Chapter 2 Parameters/Functions

Introduction

The following is a list of parameters and functions encountered within the drive. It is organized as follows:

<i>Section</i>	<i>Page</i>
Diagnostic and Utility Functions	1
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I/O Functions	19
LAN Functions	22
Protective Functions.....	30
Line Protection Module	43
Sequencer Functions	46
Source Configuration Functions	Error! Bookmark not defined.
Source Control Functions	54

Diagnostic and Utility Functions

Diagnostic and Utility Overview

The Innovation Series products contain a number of diagnostic functions. More information is available for the following topics.

- *Capture Buffer*
- *General Purpose Constants*
- *General Purpose Filters*
- *Oscillator*
- *Predefined Constants*
- *Signal Level Detector (SLD)*
- *Simulator*

Capture Buffer

The Innovation Series capture buffer is used to collect four channels of coherent data at a specified rate in the drive. It is circular, and will collect 512 samples of each data channel before overwriting the oldest data. The capture buffer can be triggered on any available variable signal in the drive by using a Boolean trigger mode or comparison to a value. It is useful for capturing drive variables for troubleshooting field problems and capturing specific drive events. The capture buffer output can be displayed in the Trend Recorder.

Function Inputs

The following table specifies the input parameters to the *Capture Buffer* function.

Parameter	Description
<i>Capture trig select</i>	Selects capture buffer trigger variable.
<i>Capture ch1 select</i>	Selects capture buffer channel #1 variable.
<i>Capture ch2 select</i>	Selects capture buffer channel #2 variable.
<i>Capture ch3 select</i>	Selects capture buffer channel #3 variable.
<i>Capture ch4 select</i>	Selects capture buffer channel #4 variable.

The following variable is also an input to the *Capture Buffer* function.

Variable	Description
<i>Capture buffer ready</i>	Enables or disables the capture buffer data collection.

Function Outputs

The following table specifies the output variable of the *Capture Buffer* function.

Variable	Description
<i>Capture buffer stat</i>	Indicates the status of the capture buffer. Possible values are: • <i>Complete</i> – Capture buffer has completed its collection of data and is disabled. • <i>Wait for trigger</i> – Capture buffer is enabled and collecting data. • <i>Post trigger capt</i> – Capture buffer has been triggered and is collecting post trigger data.
<i>Capture sample time</i>	Indicates the interval at which the capture buffer collects data based on the values of the parameters <i>Capture period</i> and <i>Capture period gain</i> . Seconds
<i>Capture triggered</i>	Indicates if the capture buffer has been triggered. True/False

Function Configuration

The following table specifies the parameters that configure the execution rate of the capture buffer.

Parameter	Description
<i>Capture period</i>	Determines the rate at which the capture

buffer collects data. Each rate in the enumeration list is based on a particular execution rate in the processor. Actual execution rates vary between each Innovation Series product. Possible values are:

- *Disable* - Disables the capture buffer from collecting data.
- *Task 1 rate* - Collects data at the fastest execution rate of the processor.
- *Task 2 rate* - Collects data at n times slower than Task 1 rate. (n Task 1's are executed every 1 Task 2).
- *Task 3 rate* - Collects data at m times slower than Task 2 rate. (m Task 2's are executed every 1 Task 3).

Note: Whenever this parameter is modified, the capture buffer must be re-enabled to collect data at the new rate.

Capture period gain Increases the collection period of the capture buffer (data is collected at a slower rate). For an integer value, n (>1), the capture buffer would collect data every nth execution of the *Capture period*.

The following table specifies the parameters that configure the capture buffer.

Parameter	Description
<i>Capture pre trigger</i>	Specifies the number of pre-trigger samples to be collected by the capture buffer.
<i>Capture trigger mode</i>	Specifies the type of comparison against the variable selected in <i>Capture trig select</i> . Note: The capture buffer will trigger when the specified comparison is satisfied. If the trigger condition is satisfied when the capture buffer is enabled, it will trigger immediately and collect post-trigger data. Possible values are: • <i>Boolean</i> - Triggers when variable is a 1. Variable in <i>Capture trig select</i> must be of Boolean type. • <i>Inverted Boolean</i> - Triggers when variable is a 0. Variable in <i>Capture trig select</i> must be of Boolean type. • <i>Equal to level</i> - Triggers when variable is equal to value in <i>Capture trig level</i>. • <i>Not equal to level</i> - Triggers when variable is not equal to value in <i>Capture trig level</i>. • <i>Greater than level</i> - Triggers when variable is greater than value in <i>Capture trig level</i>. • <i>Less than level</i> - Triggers when variable is equal to value in <i>Capture trig level</i>.
<i>Capture trig level</i>	Specifies the threshold level for level-based trigger comparisons.

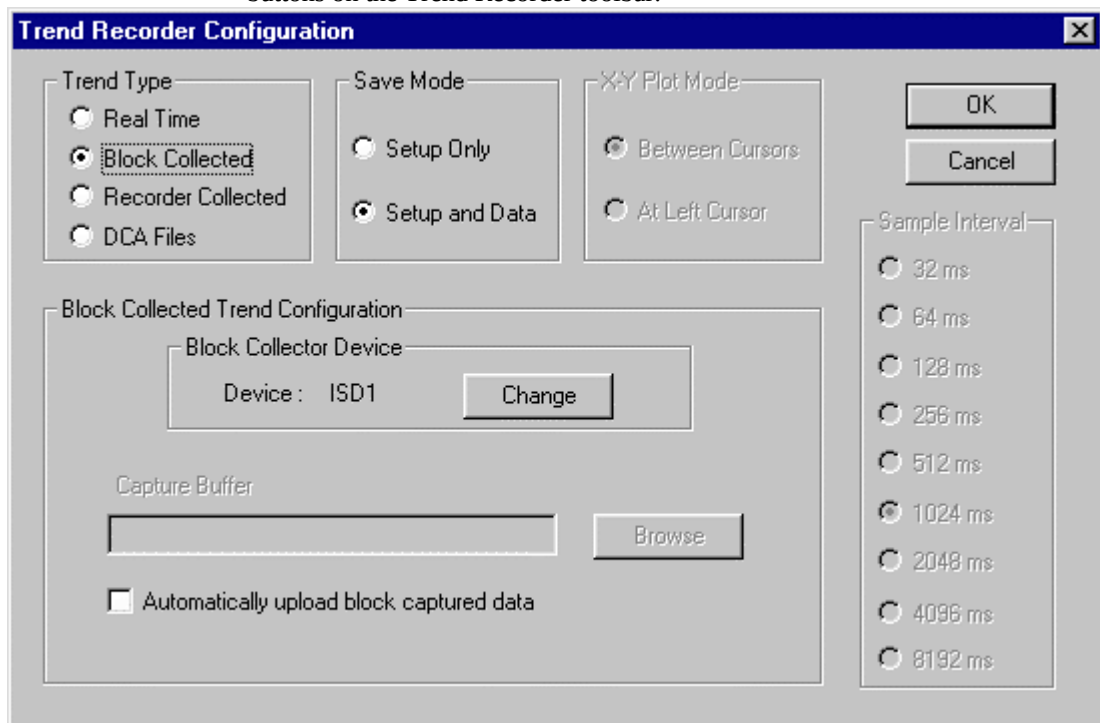
Function description

The Innovation Series product capture buffer can be accessed from the Trend Recorder in the toolbox. To enable the Trend Recorder:

- From the *View* menu, select *Trend Recorder* OR select the Trend Recorder button on the toolbar: .

To enable the Innovation Series capture buffer from the Trend Recorder:

- From the *Edit* menu, select *Configure...* OR select the *Configure* button from the Trend Recorder toolbar: .
- Select *Block Collected* as the *Trend Type* in the *Trend Recorder Configuration* dialog box and click *OK*. This enables the *Upload*  and *Edit Block*  buttons on the Trend Recorder toolbar.



- Select the *Edit Block* button from the toolbar, which brings up a block diagram that allows you to configure the capture buffer parameters described in the *Function Input and Function Configuration* sections. All of the parameter values must be sent to the drive for the capture buffer to work correctly.
- Go back to the Trend Recorder and select the *Record*  button to enable the capture buffer. The toolbox status bar should change from a “Stopped” indication:



to a “Waiting” indication:



This indicates that the capture buffer is collecting data and waiting for the trigger.

To upload the capture buffer data into the Trend Recorder, select the *Upload* button from the Trend Recorder toolbar.

Related diagrams

- Capture Buffer Configuration (Capture)

General Purpose Constants

Each Innovation Series product provides three general purpose constants. The general purpose constants allow users to place constant values in device variables. The general purpose constants are particularly useful in configuring diagnostic functions.

Function inputs

The following table specifies the input parameters of the *General Purpose Constants* function.

<i>Parameter</i>	<i>Description</i>
<i>GP Constant 1</i>	User defined constant 1
<i>GP Constant 2</i>	User defined constant 2
<i>GP Constant 3</i>	User defined constant 3

Function outputs

The following table specifies the output variables of the *General Purpose Constants* function.

<i>Variable</i>	<i>Description</i>
<i>GP Constant 1</i>	User defined constant 1
<i>GP Constant 2</i>	User defined constant 2
<i>GP Constant 3</i>	User defined constant 3

Function description

The *General Purpose Constants* function sets its output variables equal to the its input parameters:

GP Constant 1 = GP Constant 1

GP Constant 2 = GP Constant 2

GP Constant 3 = GP Constant 3

The units of the general purpose constants are determined by their use. For example, if one of the constants is used as a comparison level in a diagnostic function such as an SLD, the implied units of the constant are the internal control units of the signal against which the comparison is made. The units of the general purpose constant are not necessarily the display units of the comparison signal. For more information on the difference between display units and internal control units, see the *Language and Units Presentation* function help.

Related diagrams

- Diagnostic & Utility Functions (Diag_Util)

General Purpose Filters

Each Innovation Series product contains four general purpose filters. The general purpose filters allow users to filter signals with a specified bandwidth.

Function inputs

The following table specifies the input parameters of the *General Purpose Filters* function.

Parameter	Description
<i>GP filter 1 sel</i>	Selects input to general purpose filter 1
<i>GP filter 2 sel</i>	Selects input to general purpose filter 2
<i>GP filter 3 sel</i>	Selects input to general purpose filter 3
<i>GP filter 4 sel</i>	Selects input to general purpose filter 4

Function outputs

The following table specifies the output variables of the *General Purpose Filters* function.

Variable	Description
<i>GP filter 1 output</i>	General purpose filter 1 output
<i>GP filter 2 output</i>	General purpose filter 2 output
<i>GP filter 3 output</i>	General purpose filter 3 output
<i>GP filter 4 output</i>	General purpose filter 4 output

Function configuration

The following table specifies the configuration parameters of the *General Purpose Filters* function.

Parameter	Description
<i>GP filter 1 bndwth</i>	General purpose filter 1 bandwidth
<i>GP filter 2 bndwth</i>	General purpose filter 2 bandwidth
<i>GP filter 3 bndwth</i>	General purpose filter 3 bandwidth
<i>GP filter 4 bndwth</i>	General purpose filter 4 bandwidth

Function description

The operation of general purpose filter 1 is described here. Each of the four general purpose filters behaves in the same manner.

The input, output, and bandwidth of general purpose filter 1 are defined as follows:

Input = Variable selected by *GP filter 1 sel*

Output = *GP filter 1 output*

Bandwidth = *GP filter 1 bndwth*

The transfer functions for general purpose filter 1 is defined as follows:

$$\text{Output} = \frac{\text{Bandwidth}}{s + \text{Bandwidth}} \times \text{Input}$$

The general purpose filters run at the fastest execution rate available in the product. This is the same rate at which bridge feedbacks are collected, the fastest regulators

operate, and hardware commands are issued. The filter execution rate is generally faster than the 1-millisecond rate at which the application functions and the LAN communications occur.

Related diagrams

- Diagnostic & Utility Functions (Diag_Util)

Oscillator

Each Innovation Series product contains a diagnostic oscillator. The oscillator switches between a positive value and a negative value, spending the same amount of time at each level. The oscillator can be used as a reference signal source for test purposes.

Function outputs

The following table specifies the output variables of the *Oscillator* function.

<i>Variable</i>	<i>Description</i>
<i>Sqr wave osc output</i>	Oscillator square wave output

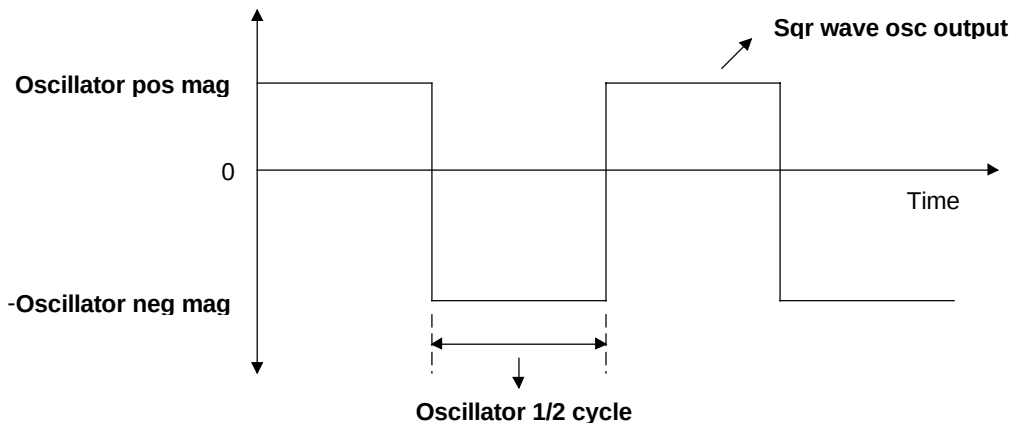
Function configuration

The following table specifies the configuration parameters of the *Oscillator* function.

<i>Parameter</i>	<i>Description</i>
<i>Oscillator neg mag</i>	Magnitude of the negative portion of oscillator output
<i>Oscillator pos mag</i>	Magnitude of the positive portion of oscillator output
<i>Oscillator 1/2 cycle</i>	Time that defines half of the oscillation period, sec
<i>Oscillator enable</i>	Enable oscillator

Function description

The *Oscillator* function produces a square wave output that switches between a positive value and a negative value. The function can be enabled or disabled via the parameter, *Oscillator enable*. The output levels and the period of the square wave are configurable. The diagram below shows how the oscillator output is generated from the configuration parameters.



Related diagrams

- Diagnostic & Utility Functions (Diag_Util)

Signal Level Detector (SLD)

Each Innovation Series product supplies three SLD channels. Each SLD does a level comparison on two inputs. The Boolean output of the SLD represents the status of the comparison. The nature of the comparison is configurable.

Function inputs

The following table specifies the input parameters of the *Signal Level Detector (SLD)* function.

Parameter	Description
<i>SLD1 input 1 select</i>	Selects SLD1 input 1 value
<i>SLD1 input 2 select</i>	Selects SLD1 input 2 value
<i>SLD2 input 1 select</i>	Selects SLD2 input 1 value
<i>SLD2 input 2 select</i>	Selects SLD2 input 2 value
<i>SLD3 input 1 select</i>	Selects SLD3 input 1 value
<i>SLD3 input 2 select</i>	Selects SLD3 input 2 value

Function outputs

The following table specifies the output variables of the *Signal Level Detector (SLD)* function.

Variable	Description
<i>SLD1 status</i>	Status of SLD1 comparison
<i>SLD2 status</i>	Status of SLD2 comparison
<i>SLD3 status</i>	Status of SLD3 comparison

Function configuration

The following table specifies the configuration parameters of the *Signal Level Detector (SLD)* function:

Parameter	Description
<i>SLD1 compare mode</i>	Type of comparison that the SLD1 function performs
<i>SLD1 sensitivity</i>	SLD1 comparison level
<i>SLD1 hysteresis</i>	SLD1 turn off deadband
<i>SLD1 pick up delay</i>	SLD1 turn on time delay, Seconds
<i>SLD1 drop out delay</i>	SLD1 turn off time delay, Seconds
<i>SLD1 input 1 abs val</i>	SLD1 input 1 mode (allows the absolute value to be used)
<i>SLD2 compare mode</i>	Type of comparison that the SLD2 function performs
<i>SLD2 sensitivity</i>	SLD2 comparison level

<i>SLD2 hysteresis</i>	SLD2 turn off deadband
<i>SLD2 pick up delay</i>	SLD2 turn on time delay, Seconds
<i>SLD2 drop out delay</i>	SLD2 turn off time delay, Seconds
<i>SLD2 input 1 abs val</i>	SLD2 input 1 mode (allows the absolute value to be used)
<i>SLD3 compare mode</i>	Type of comparison that the SLD3 function performs
<i>SLD3 sensitivity</i>	SLD3 comparison level
<i>SLD3 hysteresis</i>	SLD3 turn off deadband
<i>SLD3 pick up delay</i>	SLD3 turn on time delay, Seconds
<i>SLD3 drop out delay</i>	SLD3 turn off time delay, Seconds
<i>SLD3 input 1 abs val</i>	SLD3 input 1 mode (allows the absolute value to be used)

Function description

The following description explains the operation of SLD1. It applies equally well to SLD2 and SLD3.

Parameters *SLD1 input 1 select* and *SLD1 input 2 select* select device variables. They define the inputs for SLD1. The following table specifies how the inputs are formed based on the value of parameter *SLD1 input 1 abs val*.

<i>SLD1 input 1 abs val</i>	<i>SLD1 Input Values</i>
<i>False</i>	Input 1 = <i>SLD1 input 1 select</i> pointer value Input 2 = <i>SLD1 input 2 select</i> pointer value
<i>True</i>	Input 1 = Absolute value of <i>SLD1 input 1 select</i> pointer value Input 2 = <i>SLD1 input 2 select</i> pointer value

The parameter *SLD1 compare mode* determines the type of comparison that is performed on the two inputs. It determines how the configuration parameters *SLD1 sensitivity*, *SLD1 hysteresis*, *SLD1 pick up delay*, and *SLD1 drop out delay* are interpreted. It determines how the output *SLD1 status* is formed. The following tables specify the behavior of SLD1 for the different enumerations of *SLD1 compare mode*.

SLD1 compare mode = In1-In2>Sen

Turn on condition	(Input 1 - Input 2) > <i>SLD1 sensitivity</i>
Turn on delay time	Turn on condition must remain valid for <i>SLD1 pick up delay</i> . After the delay <i>SLD1 status</i> = True.
Turn off condition	(Input 1 - Input 2) <= (<i>SLD1 sensitivity</i> - <i>SLD1 hysteresis</i>)
Turn off delay time	Turn off condition must remain valid for <i>SLD1 drop out delay</i> . After the delay <i>SLD1 status</i> = False.

SLD1 compare mode = In1-In2<Sen

Turn on condition	$(\text{Input 1} - \text{Input 2}) < \text{SLD1 sensitivity}$
Turn on delay time	Turn on condition must remain valid for <i>SLD1 pick up delay</i> . After the delay <i>SLD1 status</i> = True.
Turn off condition	$(\text{Input 1} - \text{Input 2}) \geq (\text{SLD1 sensitivity} + \text{SLD1 hysteresis})$
Turn off delay time	Turn off condition must remain valid for <i>SLD1 drop out delay</i> . After the delay <i>SLD1 status</i> = False.

SLD1 compare mode = In1<>In2

Turn on condition	Absolute value of $(\text{Input 1} - \text{Input 2}) > \text{SLD1 sensitivity}$
Turn on delay time	Turn on condition must remain valid for <i>SLD1 pick up delay</i> . After the delay <i>SLD1 status</i> = True.
Turn off condition	Absolute value of $(\text{Input 1} - \text{Input 2}) \leq (\text{SLD1 sensitivity} - \text{SLD1 hysteresis})$
Turn off delay time	Turn off condition must remain valid for <i>SLD1 drop out delay</i> . After the delay <i>SLD1 status</i> = False.

SLD1 compare mode = In1=In2

Turn on condition	Absolute value of $(\text{Input 1} - \text{Input 2}) \leq \text{SLD1 sensitivity}$
Turn on delay time	Turn on condition must remain valid for <i>SLD1 pick up delay</i> . After the delay <i>SLD1 status</i> = True.
Turn off condition	Absolute value of $(\text{Input 1} - \text{Input 2}) > (\text{SLD1 sensitivity} + \text{SLD1 hysteresis})$
Turn off delay time	Turn off condition must remain valid for <i>SLD1 drop out delay</i> . After the delay <i>SLD1 status</i> = False.

SLD1 compare mode = In1-In2>Sen one shot

Turn on condition	$(\text{Input 1} - \text{Input 2}) > \text{SLD1 sensitivity}$
Turn on delay time	After the turn on condition is met a timer begins. The turn on condition does not need to remain valid while the timer runs. After <i>SLD1 pick up delay</i> expires <i>SLD1 status</i> =

	True.
Turn off condition	After <i>SLD1 status</i> goes True a timer begins. After <i>SLD1 drop out delay</i> expires <i>SLD1 status</i> = False. The minimum time <i>SLD1 status</i> is True is approximately 1 millisecond.
Reset condition	SLD 1 becomes active again when $(\text{Input 1} - \text{Input 2}) \leq (\text{SLD1 sensitivity} - \text{SLD1 hysteresis})$ <i>SLD1 compare mode = In1-In2<Sen one shot</i>
Turn on condition	$(\text{Input 1} - \text{Input 2}) < \text{SLD1 sensitivity}$
Turn on delay time	After the turn on condition is met a timer begins. The turn on condition does not need to remain valid while the timer runs. After <i>SLD1 pick up delay</i> expires <i>SLD1 status</i> = True.
Turn off condition	After <i>SLD1 status</i> goes True a timer begins. After <i>SLD1 drop out delay</i> expires <i>SLD1 status</i> = False. The minimum time <i>SLD1 status</i> is True is approximately 1 millisecond.
Reset condition	SLD 1 becomes active again when $(\text{Input 1} - \text{Input 2}) \geq (\text{SLD1 sensitivity} + \text{SLD1 hysteresis})$

Related diagrams

- Signal Level Detection (SLD)

Predefined Constants

Each Innovation Series product contains a number of predefined constants. These constants are available for use in a variety of functions. They are generally found on the selection lists for parameters, which select control signals.

Floating point constants

The following floating point constants are available.

- *Constant float 0.0*
- *Constant float -1.0*
- *Constant float 1.0*

Integer constants

The following integer constants are available.

- *Constant integer 0*
- *Constant integer -1*

- *Constant integer1*

Boolean constants

The following Boolean constants are available.

- *Force True*
- *Force False*

Unused constants

The Unused category of constants can be used to turn off certain product behaviors. See individual functional helps for information on the effect of the Unused constants on those functions.

The following Unused constants are available.

- *Unused float*
- *Unused integer*
- *Unused Boolean*

Simulator

The *Simulator* function allows the user to simulate the operation of the regenerative source and the ac line without applying power to the bridge, and other equipment.

Function inputs

The following table specifies the input parameters of the *Simulator* function.

Parameter	Description
<i>Simulate mode</i>	Request to run in simulation mode(yes or no). The actual change from one mode to the other will not be made unless the source is stopped.
<i>Sim line resistance</i>	Allows changing of the simulated plant resistance so that mis-matches between control settings and actual plant values can be made..
<i>Sim line inductance</i>	Allows changing of the simulated plant inductance so that mis-matches between control settings and actual plant values can be made..
<i>Sim capacitance</i>	Allows changing of the simulated plant capacitance so that mis-matches between control settings and actual plant values can be made..
<i>Sim line frequency</i>	AC line frequency in simulator mode. Note that this can be set for other than 50 or 60 hz, but should normally be set to one or the other.
<i>Sim freq slew rate</i>	Simulator frequency slew in rads/sec/sec. Setting this value to a something other than zero causes the frequency to slew continuously from nominal - .5*nominal to nominal+..25*nominal and back. This exercises the entire transient frequency range covered by the specification.
<i>Sim line voltage</i>	Simulator line to line voltage magnitude. This value

determines the magnitude of the ac line in simulator mode. It can be adjusted to simulate a low or high line condition.

<i>Sim A-N volt scale</i>	<i>Sim A-N volt scale</i> can be used to attenuate phase A line to neutral voltage in order to simulate transient line conditions. The line to neutral voltage for phase A will attenuated according to <i>Sim A-N volt scale</i> every 2.70046seconds. The duration of the transient is specified by the parameter <i>Volt short time</i> . The 2.70046sec. time was chosen so that the transient condition gradually walks through the sin wave. In order to simulate an open on phase A, set <i>Sim A-N volt scale</i> and <i>Sim B-N volt scale</i> to 1.0 and set <i>Sim C-N volt scale</i> to 0.5.
<i>Sim B-N volt scale</i>	<i>Sim B-N volt scale</i> behave identically to <i>Sim A-N volt scale</i> except that it effects phase B instead of phase A.
<i>Sim C-N volt scale</i>	<i>Sim C-N volt scale</i> behave identically to <i>Sim A-N volt scale</i> except that it effects phase C instead of phase A.
<i>A-B volt fault scale</i>	<i>A-B volt fault scale</i> simulates a line to line fault between phases A and B. The default for <i>A-B volt fault scale</i> is 0, providing no attenuation.

Function outputs

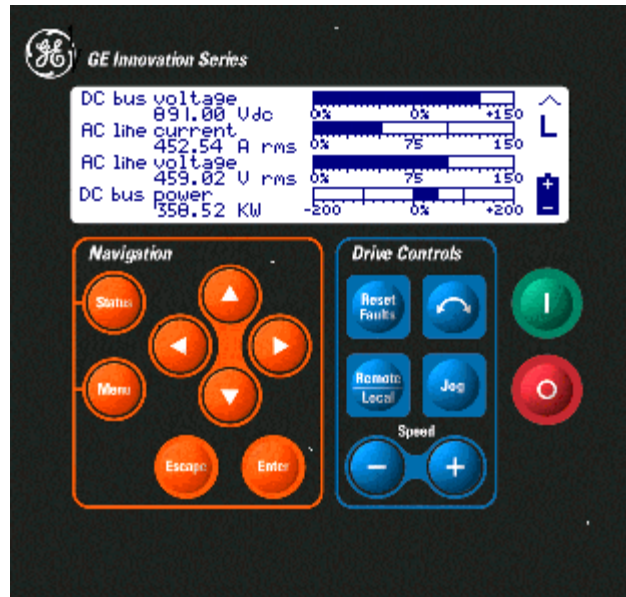
The following table specifies the output variables of the *Simulator* function.

Variable	Description
<i>Simulate mode act</i>	Simulator mode
<i>Sim A-B line voltage</i>	Simulator line to line voltage A-B
<i>Sim B-C line voltage</i>	Simulator line to line voltage B-C
<i>Sim A-N line voltage</i>	Simulator line to neutral voltage A
<i>Sim B-N line voltage</i>	Simulator line to neutral voltage B
<i>Sim C-N line voltage</i>	Simulator line to neutral voltage C
<i>Sim DC bus current</i>	Simulator dc load current
<i>Sim DC bus power</i>	Simulator dc power

General Setup Functions

Keypad Overview

The Drive Diagnostic Interface (DDI or keypad) is mounted on the door of an Innovation Series drive. The DDI provides a simple, easily accessible means for a user to set, monitor and maintain the drive locally.



The DDI provides both analog and digital representations of drive functions and values. Its keypad is logically organized into two functional groups: navigation keys and drive control keys. The Run and Stop keys are set to the side for easy access.

The operator can use the DDI to perform the following common tasks:

- Monitor dc link voltage / ac line current / ac line voltage / dc bus power
- Start/Stop the drive
- Adjust a configuration parameter
- Reset a fault condition
- Commission the drive through a wizard

Each drive has its own DDI for local control.

For the source, the Remote/Local button only has the effect to enable or disable the start button on the keypad. This button will toggle the status of *Local mode active* within the control, but has no other effect.

Related functions

Following are the DDI functions that can be modified from the toolbox:

- *Keypad Contrast Adjustment*
- *Keypad Meter Configuration*
- *Keypad Security Configuration*
- *Language Display*

Keypad Contrast Adjustment

Normally, the LCD contrast of the DDI should be adjusted at the DDI. There is a Screen Contrast Adjustment that can be selected from under the Menu screen.

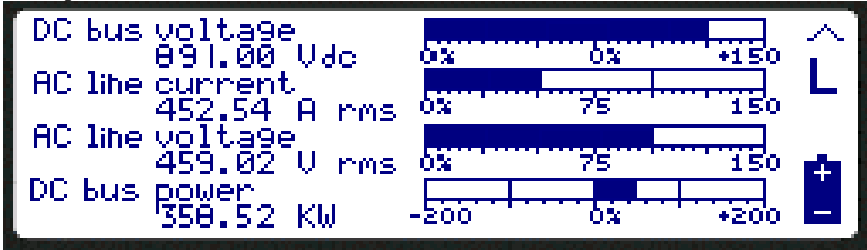
However, there may be situations where the DDI contrast is too light or too dark for the user to navigate through the menus. If this occurs, the *Keypad contrast adj* parameter may be adjusted in from the toolbox.

Function configuration

<i>Parameter</i>	<i>Description</i>
<i>Keypad contrast adj</i>	Adjusts the contrast of the DDI LCD screen. Valid values are from 0 to 63 where 63 is the darkest contrast. Setting <i>Keypad contrast adj</i> to 0 will cause the DDI to adjust the contrast to a middle value. Note: Once <i>Keypad contrast adj</i> has been modified in the toolbox and then saved in the drive, a hard reset must be performed for the user to see their modification to the contrast reflected in the DDI.

Keypad Meter Configuration

The DDI Status screen has are four animated meters and associated text that display drive performance information.



The variables, displayed by the meters and the meter ranges, can be modified by configuring the following parameters.

Function configuration

<i>Parameter</i>	<i>Description</i>
<i>Keypad meter 1 sel</i>	Selects a floating-point variable that is displayed in Meter #1 on the DDI Status screen.
<i>Keypad meter 2 sel</i>	Selects a floating-point variable that is displayed in Meter #2 on the DDI Status screen.
<i>Keypad meter 3 sel</i>	Selects a floating-point variable that is displayed in Meter #3 on the DDI Status screen.
<i>Keypad meter 4 sel</i>	Selects a floating-point variable that is displayed in Meter #4 on the DDI Status screen.
<i>Keypad meter 1 range</i>	Selects the bar graph meter scaling for Meter #1. Possible values are as follows (note that all bar graphs are scaled in percent (%)): • 0 to +100 • -100 to +100 • 0 to +150 • -150 to +150 • 0 to +200 • -200 to +200 • 0 to +300

- -300 to +300

<i>Keypad meter 2 range</i>	Selects the bar graph meter scaling for Meter #2. See <i>Keypad meter 1 range</i> for possible values.
<i>Keypad meter 3 range</i>	Selects the bar graph meter scaling for Meter #3. See <i>Keypad meter 1 range</i> for possible values.
<i>Keypad meter 4 range</i>	Selects the bar graph meter scaling for Meter #4. See <i>Keypad meter 1 range</i> for possible values.

Note: When changing DDI meter configuration from the toolbox, you must first save the modified parameters to the drive. Then you must press the **Menu** button, then the **Status** button on the DDI to cause the meters on the Status screen to update.

Keypad Security Configuration

The DDI contains security controls that can protect the drive from being operated or reconfigured by unauthorized personnel. These security controls can be modified from either the toolbox or the DDI; however, the controls are password protected in the DDI.

Function configuration

<i>Parameter</i>	<i>Description</i>
<i>Keypad privilege</i>	Selects the privilege level in the DDI. Possible levels are: • <i>Read only</i> - Disables both drive controls and configuration functions. Allows user to view but not edit parameters. • <i>Operate & read only</i> - Enables drive controls, but disables configuration functions. Allows user to view but not edit parameters. • <i>Configure & operate</i> - Enables both drive controls and configuration functions. See below for full list of enabled functions for each level.
<i>Keypad password</i>	Sets the 5-digit password value for the DDI. When a user attempts to modify the Keypad security configuration from the DDI, he will be prompted to enter a password. If the entered password does not match the value in <i>Keypad password</i> , the user will not be permitted to modify the security configuration (i.e. <i>Keypad privilege</i> and <i>Keypad password</i>).

Function description

A list of all DDI functions is displayed in the table below. Available functions for each privilege level are checked.

Note that for regenerative and non-regenerative sources, the following functions are not meaningful and therefore the associated keypad buttons are non-functional: Change direction, Jog, Speed Increment and Speed Decrement.

Keypad Function	Privilege Level		
	Read Only	Operate & read only	Cofigure & operate
Drive control functions			
Stop	✓	✓	✓
Start		✓	✓
Reset faults	✓	✓	✓
Change direction		✓	✓
Remote/Local		✓	✓
Jog		✓	✓
Speed Increment		✓	✓
Speed Decrement		✓	✓
Menu functions			
Status button	✓	✓	✓
Menu button	✓	✓	✓
Navigation buttons (Arrows, Esc, Enter)	✓	✓	✓
Display Active Faults	✓	✓	✓
Display Fault History	✓	✓	✓
View Parameters	✓	✓	✓
Edit Parameters			✓
View Variables	✓	✓	✓
Wizards			✓
Adjust Screen Contrast	✓	✓	✓
Display Firmware Version	✓	✓	✓
Display Hardware Information	✓	✓	✓
Save Parameters to Backup			✓
Restore Parameters from Backup			✓
Compare Current Parameters to Backup	✓	✓	✓
View Overrides	✓	✓	✓

Note: When changing DDI security configuration from the toolbox, you must first save the modified parameters to the drive. Then you must switch between the Menu and Status screens for the password and privilege level to update.

Language and Units Presentation

The presentation of the Innovation Series product in the toolbox and DDI can be customized. The presentation can be configured using the following parameters:

- *Language*
- *Display units*

In regions in which English is not the primary language, the Innovation Series product provides a choice of two languages, English and the indigenous language. The presentation's language is determined by the parameter *Language* setting

Parameters and variables in the Innovation Series product can be displayed in different unit systems. The display units are chosen by the parameter, *Display units*. Three different unit systems are available:

- *Imperial (English)*
- *Metric (SI)*
- *Native (Platform)*

If *Display units* is set to *Native (Platform)*, then values are displayed in the same units that the internal control uses. The following table specifies some of the unit system differences.

Display units	Length	Power	Torque	Flux
<i>Imperial (English)</i>	Feet	Horsepower	Foot-pounds	Volts/hertz
<i>Metric (SI)</i>	Meters	Kilowatts	Newton-meters	Volts/hertz
<i>Native (Platform)</i>	Meters	Watts	Newton-meters	Webers

Language Display

The DDI can display its menu and status information in an alternate language as long as the keypad has been configured correctly.

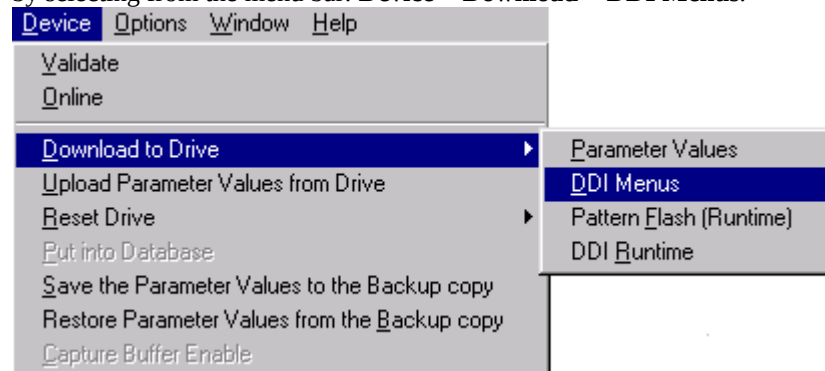
Note: *Presently this function is not yet operational.*

Function configuration

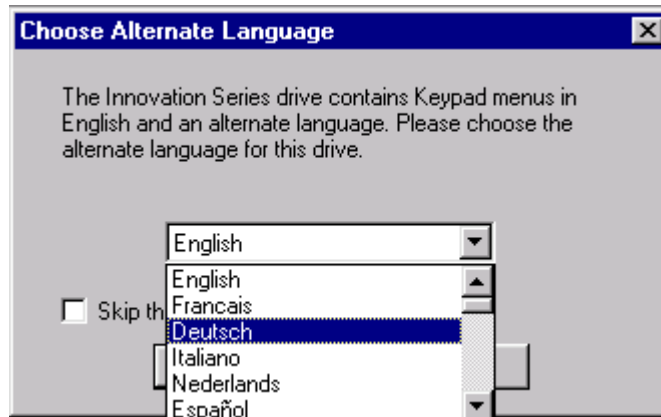
Parameter	Description
<i>Language</i>	Selects the language in which to display all information in the DDI. Possible selections are: <i>English</i> - Displays DDI text in English. <i>Native</i> - Displays DDI text in the native language that is specified when DDI Menus are downloaded from the toolbox (see below).

Function description

To display the DDI text in a language other than English, the user must first download the appropriate DDI Menus. This operation is performed from the toolbox by selecting from the menu bar: **Device > Download > DDI Menus**.



The user will then be prompted to select an alternate language to download to the DDI.



The toolbox will then build the DDI Menu file. The user can then download to the DDI.

Once the download is complete, the user can then modify the *Language* parameter to the desired value. The DDI will display its text in the selected language the next time its screen is updated.

I/O Functions

Analog and Digital I/O Testing

The *Analog and Digital I/O Testing* function is intended for factory use only.

Function configuration

The following table specifies the configuration parameters for the *Analog and Digital I/O Testing* function.

Parameter	Description
<i>I/O test mode req</i>	Hardware I/O test request.
<i>Simulate mode</i>	Simulator mode request.

Both *I/O test mode req* and *Simulate mode* must be *True* for the *Analog and Digital I/O Testing* function to be active. *I/O test mode* is *True* when the function is active.

Analog inputs

The following table specifies the signals available for testing the analog inputs.

Variable	Description
<i>Analog input 1 volts</i>	Voltage of analog input 1 source. DC volts
<i>Analog input 2 volts</i>	Voltage of analog input 2 source. DC volts

Digital inputs

The following table specifies the signals available for testing the digital inputs.

Variable	Description
<i>Digital input 1 test</i>	Unfiltered value of digital input 1.
<i>Digital input 2 test</i>	Unfiltered value of digital input 2.
<i>Digital input 3 test</i>	Unfiltered value of digital input 3.

<i>Digital input 4 test</i>	Unfiltered value of digital input 4.
<i>Digital input 5 test</i>	Unfiltered value of digital input 5.
<i>Digital input 6 test</i>	Unfiltered value of digital input 6.

Hi Fi counters

The following table specifies the signals available for testing the high fidelity VCO counters.

<i>Variable</i>	<i>Description</i>
<i>VCO 1 unfiltered</i>	VCO 1 counter value.
<i>VCO 2 unfiltered</i>	VCO 1 counter value.
<i>VCO 3 unfiltered</i>	VCO 1 counter value.

Local and system fault strings

The following table specifies the signals available for testing the local and system fault strings.

<i>Variable</i>	<i>Description</i>
<i>Local fault test</i>	Unfiltered value of local fault string.
<i>System fault test</i>	Unfiltered value of system fault string.

Contactor status

The following table specifies the signals available for testing the main contactor status input.

<i>Variable</i>	<i>Description</i>
<i>MA cont test mode</i>	Unfiltered value of main contactor status.

DAC and meter outputs

The following table specifies the parameters that configure the analog output (DAC) and meter output tests.

<i>Parameter</i>	<i>Description</i>
<i>Analog out 1 test</i>	DAC 1 output voltage. DC volts
<i>Analog out 1 test</i>	DAC 2 output voltage. DC volts
<i>Analog out 1 test</i>	DAC 3 / Meter 1 output voltage. DC volts
<i>Analog out 1 test</i>	DAC 4 / Meter 2 output voltage. DC volts
<i>Analog meter 3 test</i>	Meter 3 output voltage. DC volts
<i>Analog meter 4 test</i>	Meter 4 output voltage. DC volts

Relay outputs

The following table specifies the parameters that configure the relay output test.

<i>Parameter</i>	<i>Description</i>
<i>Relay 1 test</i>	Relay 1 output.
<i>Relay 2 test</i>	Relay 2 output.
<i>Relay 3 test</i>	Relay 3 output.

Related diagrams

- Analog and Digital I/O Testing (HWIO_Tst)

Analog Inputs/Outputs and Mapping

Analog Inputs

Two bipolar (+/- 10 volts) analog inputs are available at the terminal board (ATB). Jumpers on the BAIA board connect a burden resistor that allow these inputs to be used for 4-20 ma references.

Analog in 1 offset and *Analog in 2 offset* provide a voltage offset adjustment. *Analog in 1 gain* and *Analog in 2 gain* can be used to scale the inputs from volts to appropriate application units. *Analog in 1 filter* and *Analog in 2 filter* provide first-order signal softening at *Analog input 1* and *Analog input 2*.

Loss of 4-20 ma signal can be configured by selecting a lower threshold *Analog in 1 flt lev* and *Analog in 2 flt lev* and then selecting the appropriate fault type, *Analog in 1 flt mode* and *Analog in 2 flt mode*.

Analog Outputs

Two bipolar (+/- 10 volts) DAC outputs are available at the terminal board (ATB). The signal to be output is selected by *Analog out 1 select*. This signal can be offset by *Analog out 1 offset* using the same units as the signal to be output. The signal is scaled for output by setting *Analog out 1 scale* to the value, which shall produce +10 volts. The second DAC is configured in a similar manner.

Meters:

Four bipolar (+/- 10 volts) meter drivers are available for use with the optional meter assembly. This assembly is connected to the drive at connector J8 on the backplane.

The signal to be metered is selected by *Analog meter 1 sel*. This signal can be offset by *Meter 1 offset* using the same units as the signal to be metered. The signal is scaled for output by setting *Analog meter 1 scale* to the value, which shall produce +10 volts. *Meter 1 mode* is used to accommodate both 0 - +10 volt meters and -10 - +10 volt meters. *Analog meter 1 scale* is unaffected by *Meter 1 mode*. The remaining three meters are configured similarly.

Related diagrams

- Analog Inputs / Outputs & Mapping (HWIO_Ana)

Digital Inputs/Outputs and Mapping

Digital inputs and outputs provide an interface between the outside world and the control. the ATB (terminal board) provides six general purpose digital inputs. Three dry contact relays and one solid state relay driver are provided as outputs. System and Local fault strings provide start and trip interlocks to the control.

Isolated digital inputs are listed with their associated terminal board points. A filter is provided to debounce a noisy input signal. The filter should be set to zero in most instances, since the hardware provides a level of debounce conditioning. The variables *Digital input 1* through *Digital input 6* indicate the logical state of each

digital input and are used to interface functions in the drive that require a Boolean signal.

Each relay output may be used by setting the parameters *Relay 1 select* through *Relay 3 select* to the variables whose logical states are desired to drive the corresponding relay. The associated terminal board points are shown for output terminals of each relay. The variables *Relay 1 state*, *Relay 2 state*, and *Relay 3 state* indicate the status of the relay coils (energized or not).

Relay four is a solid-state relay driver that should be used to drive a 24 Vdc, 10mA relay. The relay driver output may be used by setting the parameter *SS relay driver sel* to the variable whose logical state is desired to drive the relay. *Solid state relay* indicates the status of the relay driver.

A pilot relay is provided for controlling a main contactor. This contactor is controlled through source sequencing.

Contactor status feedback is available *MA contactor closed*.

Related diagrams

- Digital Inputs / Outputs & Mapping (HWIO_Dig)

LAN Functions

LAN Overview

Information is available for the following LAN topics:

- *Frame Phaselock Loop*
- *LAN Configuration and Health*
- *LAN Signal Map*

Frame Phaselock Loop

The *Frame Phaselock Loop* function supports the ability to synchronize the execution of the Innovation Series Drive control firmware with the communication frame of the product application interface. This feature is available only for those interface that support synchronous communications such as ISBus.

Function outputs

The following table specifies the published output variables of the *Frame Phaselock Loop* function.

Variable	Description
<i>Frame PLL OK status</i>	Boolean signal indicating the lock status of the <i>Frame Phaselock Loop</i> .
<i>FPLL Phase error</i>	Phase error signal for the <i>Frame Phaselock Loop</i> . Scaling is per-unitized so that unity corresponds to the full frame period; signal values range from minus one-half to plus one-half.
<i>FPLL Freq Output</i>	Frequency adjustment output signal for the <i>Frame</i>

Phaselock Loop. Scaling is per-unitized so that unity corresponds to the full frame period; signal values range from minus output limit to plus output limit.

Function configuration

The following table specifies configuration parameters related to the *Frame Phaselock Loop* function.

Parameter	Description
<i>Network interface</i>	Network interface type. Specifies one of the following interface types: • No interface • ACL dual port memory (synchronous operation supported) • ISBus (synchronous operation supported) • DRIVENET - Optional LAN modules such as Genius & Profibus
<i>LAN frame time</i>	Expected communication frame period. Allowed frame periods are 1, 2, 4, and 8 milliseconds.

Function description

Configuration of the *Frame Phaselock Loop* function is handled completely by the product. Appropriate user selections of *Network interface* activate the function, and user specification of *LAN frame time* sets the nominal period.

The Boolean variable *Frame PLL OK statu* indicates the status of the *Frame Phaselock Loop*. The asserted state indicates that the function has been activated and that lock status has been validated. The unasserted state indicates either that the function is not activated, or that lock status is not validated.

The *FPLL Phase error* signal reflects the phase error when valid phase information has been extracted from the interface. A signal value of zero indicates either zero phase error or invalid phase information. Scaling is so that one per-unit phase error represents a full communication frame period.

The *FPLL Freq Output* signal is the frequency adjustment output of the function; the authority of the function to modify away from nominal frequency is strictly limited. When the function is not activated, the *FPLL Freq Output* signal is zero. When the function is activated, but no valid phase information is detected, then *FPLL Freq Output* maintains its last valid calculated value.

When phaselock is achieved, *Frame PLL OK status* is asserted, *FPLL Phase error* is at a zero-mean steady-state value, and *FPLL Freq Output* is at a non-zero, but very small, steady-state value. When the *Frame Phaselock Loop* has been requested by configuration but phaselock is not achieved, then *Frame PLL not OK* is shown.

LAN Configuration and Health

The information below describes the configuration of the primary signal interface between the Innovation Series device and the application layer interface. The application layer may consist of an embedded ACL card, a direct LAN interface card, or an application-level ISBus serial bus.

Configuration parameters

The following table specifies the configuration parameters of the *LAN Configuration and Health* function.

Parameter	Description
<i>Network interface</i>	Network interface type. Specifies one of the following interface types: • No interface • ACL dual port memory • ISBus • DRIVENET – Other optional LAN modules such as Genius and Profibus
<i>LAN frame time</i>	Expected communication frame period. Allowed frame periods are 1, 2, 4, and 8 milliseconds.
<i>LAN fbk avg time</i>	Period over which feedback signals are sequentially averaged. The <i>LAN Signal Map</i> help topic describes which feedback signals are averaged. If <i>LAN fbk avg time</i> is zero, no averaging occurs.
<i>LAN cmds inhibit</i>	Disables LAN references, forcing the signal interface to operate in feedback-only mode. Local images of reference signals are set to zero (0.0) or False.
<i>LAN trips inhibit</i>	Disables LAN heartbeat trip fault (<i>LAN heartbeat trip</i>), and enable the corresponding alarm (<i>LAN heartbeat alarm</i>).
<i>LAN heartbeat time</i>	Period within which transition must be detected in the LAN heartbeat signal (<i>Heartbeat ref, lan</i>) to satisfy the local heartbeat timeout check.
<i>Sys ISBus node #</i>	ISBus node for the Innovation Series Drive device. Each device on the ISBus bus should be assigned a unique node between 1 and 31.
<i>LAN parameter 1 through LAN parameter 16</i>	These parameters are used only by optional LAN modules and are specific to those modules. Such items as baud rate and device number are configured via these parameters. Please see the documentation for the specific LAN module for detailed information.

Diagnostic variables

The following table specifies variables, which indicate the LAN health and status for the *LAN Configuration and Health* function.

Variable	Description
<i>LAN connection ok</i>	Indicates that the health of the LAN connection is good, so that the LAN watchdog function is satisfied.
<i>LAN commands OK</i>	Indicates that the health of the LAN references is good, based upon detection of two successive <i>LAN connection ok</i> indications.
<i>Heartbeat ref, lan</i>	LAN heartbeat signal that proceeds from the application layer to the local device, used locally for (<i>LAN heartbeat trip</i>) and (<i>LAN heartbeat alarm</i>) detection, and as the source of the reflected <i>Heartbeat fbk, lan</i> signal.

<i>Heartbeat fbk, lan</i>	Local device reflection of the <i>Heartbeat ref, lan</i> signal that is sent back to the application layer.
<i>Sys ISBus error cnt</i>	Counter signal which provides an indication of the rate of occurrence of ISBus fault conditions.
<i>Sys ISBus error reg</i>	Bit-coded value of the last ISBus fault detected; each bit indicates a particular ISBus fault seen by the control.
<i>Frame PLL OK status</i>	Boolean signal indicating the lock status of the <i>Frame Phaselock Loop</i> .
<i>FPLL Phase error</i>	Phase error signal for the <i>Frame Phaselock Loop</i> . Scaling is per-unitized so that unity corresponds to the full frame period; signal values range from minus one-half to plus one-half.
<i>FPLL Freq Output</i>	Frequency adjustment output signal for the <i>Frame Phaselock Loop</i> . Scaling is per-unitized so that unity corresponds to the full frame period; signal values range from minus output limit to plus output limit.

Function description

Determination of the integrity of the LAN interface involves several communication layers and may vary depending upon the specific communication options in use. Two levels of validation are available to the Innovation Series Drive: “Lan watchdog” and “Lan heartbeat”. Status information is conveyed to the user and/or application by status signals and fault declarations.

The “Lan watchdog” function describes a set of mechanisms by which the drive determines the status of the connection between DSPX and the module immediately “above” the drive in the LAN hierarchy. For Dual-Port RAM interfaces, used for an embedded ACLA controller and for a direct LAN interface, the watchdog takes the form of a handshake protocol by which the drive determines the presence of a minimum level of intelligence on the host on the “Lan side” of the shared memory. For ISBus interfaces, such as that utilized by a remote or embedded ACLA controller, the watchdog reflects the reception of ISBus frame synchronization codes. The watchdog function’s immediate authority is limited to alarms and status variables; however, the status information plays a functional role in the interface management. Note that the watchdog offers no information as to the status of the Lan connection. The Lan connection may be supported beyond the immediate interface to DSPX. In fact, many “device networks” offer no means of determining basic network health.

The “Lan heartbeat” function is visible to the user. The function uses published signal map channels, and is available for use by the application. It provides the signal a way to “loop back” a signal between the drive and any level in the Lan hierarchy so that a higher-level controller can validate the entire connection pathway, including the drive itself. Locally, the drive can be configured to generate a trip or alarm if the heartbeat reference signal fails to transition within a configurable period of time. The heartbeat offers the most robust validation options from a system perspective, although it offers the least information relative to the location of a detected problem.

The *System ISBus error* alarm is triggered when an ISBus fault is detected in the DSPX control. The variable *Sys ISBus error reg* contains the bit-coded value of the last ISBus fault detected; each bit indicates a particular ISBus fault seen by the

control. The variable, *Sys ISBus error cnt*, increments upon fault detection. After initialization of the interface, the alarm is expected to go off periodically.

The *Frame PLL not OK* alarm occurs when phase-lock between the DSPX control and the System ISBus or (local ACL) is not assured. Detection of the fault is enabled when the parameter *Network interface* is configured to select an interface for which synchronized operation is supported. The presence of this alarm indicates that data coherency is compromised. Status of the *Frame Phaselock Loop* function can be observed via the signals *Frame PLL OK status*, *FPLL Phase error*, and *FPLL Freq Output*.

LAN Signal Map

The information below describes the primary signal interface between the Innovation Series Drive and the product application layer interface. The application layer may consist of an embedded ACL card, a direct LAN interface card, or an application-level ISBus serial bus.

The *LAN Signal Map* is a fixed signal map, which defines dedicated registered communication channels for specific signals. It is defined in terms of paired reference and feedback pages, which are of the same physical size. The internal data organization of the reference and feedback pages may differ. The standard Innovation Series signal map page consists of eight 32-bit elements.

Each 32-bit element in the *LAN Signal Map* is assigned a data type. The following data types are used.

- Single precision floating point, IEEE 754 format (23-bit mantissa, 8-bit exponent, 1-bit sign).
- Two's complement integer.
- Individual 1-bit Boolean signals.

LAN References

The following table specifies the *LAN Signal Map* reference signals.

<i>Page</i>	<i>Element</i>	<i>Signal</i>	<i>Data Type</i>	<i>Description</i>
1	1		Boolean bits	Boolean requests. See table below for definition of request bits.
1	2	<i>LAN Iy ref</i>	Floating point	Lan reference for reactive current. See <i>Reactive Current Reference</i> function.
1	3	<i>LAN Iy fbk</i>	Floating point	Lan feedback for reactive current. See <i>Reactive Current Reference</i> function.
1	4-6	Unused		
1	7	<i>GP lan ref 1</i>	Floating point	General purpose reference that can be used by a number of functions.

1	8	<i>GP lan ref 2</i>	Floating point	General purpose reference that can be used by a number of functions.
2	1-6	Unused		
2	7	<i>GP lan ref 3</i>	Floating point	General purpose reference that can be used by a number of functions.
2	8	<i>GP lan ref 4</i>	Floating point	General purpose reference that can be used by a number of functions.

The following table specifies the *LAN Signal Map* request bits that appear in Page 1, Element 1 of the reference signal map.

Bit	Signal	Description
0	<i>Heartbeat ref, lan</i>	Heartbeat signal to validate LAN health.
1	<i>Fault reset req, lan</i>	Request to reset drive faults. Functionality is always enabled.
2	<i>Trip request, lan</i>	Request to trip the drive. Functionality is always enabled.
3	<i>Alarm request, lan</i>	Request to declare an alarm in the drive. Functionality is always enabled.
4-9	Unused	
10	<i>X stop request, lan</i>	Request to perform an X stop in the drive. Functionality is always enabled.
11-23	Unused	
24	<i>GP lan req bit 1</i>	General purpose request that can be used by a number of functions.
25	<i>GP lan req bit 2</i>	General purpose request that can be used by a number of functions.
26	<i>GP lan req bit 3</i>	General purpose request that can be used by a number of functions.
27	<i>GP lan req bit 4</i>	General purpose request that can be used by a number of functions.
28	<i>GP lan req bit 5</i>	General purpose request that can be used by a number of functions.
29	<i>GP lan req bit 6</i>	General purpose request that can be used by a number of functions.
30	<i>GP lan req bit 7</i>	General purpose request that can be used by a number of functions.
31	<i>GP lan req bit 8</i>	General purpose request that can be used by a number of functions.

LAN Feedbacks

Several LAN feedback signals are averaged versions of internal drive signals. The signals that fall in this category appear in dedicated floating point feedback channels. The averaging is sequential (not rolling) and the averaging time is specified by parameter *LAN fbk avg time*.

The following table specifies the *LAN Signal Map* feedback signals.

Page	Element	Signal	Data Type	Description
1	1		Boolean bits	Boolean feedbacks. See table below for definition of feedback bits.
1	2	<i>Fault number</i>	Integer	Number of active fault. Priority is given to trip faults over alarms, and to the earliest detected fault.
1	3	<i>AC line current, lan</i>	Floating point	Averaged AC line current.
1	4	<i>AC line voltage, lan</i>	Floating point	Averaged Avg line voltage mag.
1	5	<i>DC bus voltage, lan</i>	Floating point	Averaged DC bus voltage.
1	6	<i>DC bus power, lan</i>	Floating point	Averaged DC bus power
1	7	<i>GP lan fbk reg 1</i>	Floating point	General purpose feedback selected by <i>GP lan fbk reg 1 sel</i> .
1	8	<i>GP lan fbk reg 2</i>	Floating point	General purpose feedback selected by <i>GP lan fbk reg 2 sel</i> .
2	1	<i>AC line freq, lan</i>	Floating point	Averaged line frequency AC line frequency.
2	2	<i>AC line vars, lan</i>	Floating point	Averaged line VARs , Volt amps reactive
2	3-6	Unused		
2	7	<i>GP lan fbk reg 3</i>	Floating point	General purpose feedback selected by <i>GP lan fbk reg 3 sel</i> .
2	8	<i>GP lan fbk reg 4</i>	Floating point	General purpose feedback selected by <i>GP lan fbk reg 4 sel</i> .

The general purpose feedback signals *GP lan fbk reg 1*, ..., *GP lan fbk reg 4* are not averaged. The following parameters are used to select the general purpose feedbacks.

- *GP lan fbk reg 1 sel*
- *GP lan fbk reg 2 sel*

- *GP lan fbk reg 3 sel*
- *GP lan fbk reg 4 sel*

The following table specifies the *LAN Signal Map* feedback bits that appear in Page 1, Element 1 of the feedback signal map.

Bit	Signal	Description
0	<i>Heartbeat fbk, lan</i>	Heartbeat signal to validate LAN health.
1	<i>No faults active</i>	No trip faults or alarms are active in the drive.
2	<i>Trip fault active</i>	Trip fault is active in the drive.
3	<i>Local fault string</i>	Local hardware permissive fault is active in the drive.
4	<i>System fault string</i>	System hardware permissive fault is active in the drive.
5	<i>Ready to run</i>	Drive is ready and will respond to a run request.
6	<i>Bridge is on</i>	Bridge power is enabled.
7	<i>Running</i>	Drive is running; References and regulators are enabled.
8-9	Unused	
10	<i>X stop active</i>	Result of X stop requests.
11-23	Unused	
24	<i>GP lan fbk bit 1</i>	General purpose feedback selected by <i>GP lan fbk bit 1 sel</i> .
25	<i>GP lan fbk bit 2</i>	General purpose feedback selected by <i>GP lan fbk bit 2 sel</i> .
26	<i>GP lan fbk bit 3</i>	General purpose feedback selected by <i>GP lan fbk bit 3 sel</i> .
27	<i>GP lan fbk bit 4</i>	General purpose feedback selected by <i>GP lan fbk bit 4 sel</i> .
28	<i>GP lan fbk bit 5</i>	General purpose feedback selected by <i>GP lan fbk bit 5 sel</i> .
29	<i>GP lan fbk bit 6</i>	General purpose feedback selected by <i>GP lan fbk bit 6 sel</i> .
30	<i>GP lan fbk bit 7</i>	General purpose feedback selected by <i>GP lan fbk bit 7 sel</i> .
31	<i>GP lan fbk bit 8</i>	General purpose feedback selected by <i>GP lan fbk bit 8 sel</i> .

The following parameters are used to select the general purpose feedback bits.

- *GP lan fbk bit 1 sel*
- *GP lan fbk bit 2 sel*
- *GP lan fbk bit 3 sel*
- *GP lan fbk bit 4 sel*

- *GP lan fbk bit 5 sel*
- *GP lan fbk bit 6 sel*
- *GP lan fbk bit 7 sel*
- *GP lan fbk bit 8 sel*

Protective Functions

The PWM source provides many standard Innovation Series platform protective functions, as well as source specific protections. Because of protective conditions, the source to shows specific *faults*, which can be used to guide diagnosis and repair as applicable. Faults are either *trip faults*, which cause the source to trip, or *alarm faults* which do not trip the source, but instead show the abnormal condition for warning or diagnostic record reasons.

There are literally hundreds of possible faults in the extensively monitored source. For orientation purposes, note that faults generally fall into the following classes:

- AC Line Faults
- Bridge Feedback Faults
- Bridge Hardware Faults
- Bridge Thermal Faults
- I/O Faults
- LAN Communications Faults
- Platform Execution Faults
- Sequencer Faults
- Source Control Faults

Some of the classes consist only of standard Innovation Control faults, or source specific, but some consist of both. Details are provided in the specific fault code help documentation.

Custom User Faults

Each Innovation Series product can configure two fault circuits. The trip faults *Customer use NC flt* and *Customer use NO flt* are triggered by input signals, which are the states of the fault circuits. *Customer use NC flt* occurs when the normally closed circuit is open. *Customer use NO flt* occurs when the normally open circuit is closed.

Function inputs

The following table specifies the input parameters of the *Custom User Faults* function.

<i>Parameter</i>	<i>Description</i>
<i>User NC fault sel</i>	Selects the source of the normally closed circuit input.
<i>User NO fault sel</i>	Selects the source of the normally open circuit input.

Faults and alarms

The following table specifies the faults and alarms declared by the *Custom User Faults* function.

Fault/Alarm	Description
<i>Customer use NC flt</i>	Trip fault that occurs when the normally closed circuit input is <code>False</code> , indicating that the circuit is open
<i>Customer use NO flt</i>	Trip fault the occurs when the normally open circuit input is <code>True</code> , indicating that the circuit is closed

Function description

The parameters *User NC fault sel* and *User NO fault sel* generally select digital inputs (variables *Digital input 1*, ..., *Digital input 6*) or general purpose LAN requests (variables *GP lan req bit 1*, ..., *GP lan req bit 8*). The custom user faults may be disabled by selecting **Unused** for the input parameters.

Ground Fault Protection (Fast)

The *Ground Fault Protection (Fast)* tests the phase currents to verify that there is no ground current in the system.

Function inputs

The following table specifies the input parameters of the *Ground Fault Protection (Fast)* function.

Parameter	Description
<i>Phase A current</i>	Phase A current feedback. Amps
<i>Phase B current</i>	Phase B current feedback. Amps
<i>Phase C current</i>	Phase C current feedback. Amps

Function outputs

The following table specifies the output variables of the *Ground Fault Protection (Fast)* function.

Variable	Description
<i>Gnd current, coarse</i>	Ground current, filtered. Amps

Function configuration

The following table specifies the configuration parameters for the *Ground Fault Protection (Fast)* function.

Parameter	Description
<i>Gnd flt coarse trip</i>	Current level at which the <i>Gnd flt, coarse</i> trip fault occurs. Amps

Faults and alarms

The following faults and alarms are declared by the *Ground Fault Protection (Fast)* function.

<i>Fault / Alarm</i>	<i>Description</i>
<i>Gnd flt, coarse</i>	Occurs when <i>Gnd current, coarse</i> > <i>Gnd flt coarse trip</i> .

Function description

Gnd current, coarse is determined by summing and filtering the three phase currents *Phase A current*, *Phase B current*, and *Phase C current*.

The configuration parameter *Gnd flt coarse trip* can be set to a default value by running the *Ground Fault Setup*.

Ground Fault Protection (Slow)

The *Ground Fault Protection (Slow)* tests the phase currents to verify that there is no ground current in the system.

Function inputs

The following table specifies the input parameters of the *Ground Fault Protection (Slow)* function.

<i>Parameter</i>	<i>Description</i>
<i>Phase A current</i>	Phase A current feedback. Amps
<i>Phase B current</i>	Phase B current feedback. Amps
<i>Phase C current</i>	Phase C current feedback. Amps

Function outputs

The following table specifies the output variables of the *Ground Fault Protection (Slow)* function.

<i>Variable</i>	<i>Description</i>
<i>Ground current</i>	Ground current, averaged and filtered. RMS amps

Function configuration

The following table specifies the configuration parameters for the *Ground Fault Protection (Slow)* function.

<i>Parameter</i>	<i>Description</i>
<i>Gnd flt trip level</i>	Current level at which the <i>Gnd flt, filtered</i> trip fault occurs. RMS amps
<i>Gnd flt alm level</i>	Current level at which the <i>Gnd flt alarm</i> occurs. RMS amps
<i>Gnd flt alm clr lvl</i>	Current level at which the <i>Gnd flt alarm</i> clears. RMS amps

Faults and alarms

The following faults and alarms are declared by the *Ground Fault Protection (Slow)* function.

<i>Fault / Alarm</i>	<i>Description</i>
<i>Gnd flt, filtered</i>	Occurs when <i>Ground current</i> > <i>Gnd flt trip level</i> .
<i>Gnd flt alarm</i>	Occurs when <i>Ground current</i> > <i>Gnd flt alm level</i> .

Clears when *Ground current* < *Gnd flt alm clr lvl*.

Function description

Ground current is determined by summing, averaging, and filtering the three phase currents: *Phase A current*, *Phase B current*, and *Phase C current*.

The configuration parameters *Gnd flt trip level*, *Gnd flt alm level*, and *Gnd flt alm clr lvl* can be set to default values by running the *Ground Fault Setup*.

Hardware Fault Strings

Each Innovation Series product provides a hardwired, fail safe circuit to turn off bridge power and to shut down its control. The circuit consists of two independent isolated inputs: the local and system fault strings. The loss of either input results in the shutdown of the power bridge and control.

Diagnostic variables

The following tables specifies the *Hardware Fault Strings* diagnostic variables.

Variable	Description
<i>Local fault string</i>	State of the local fault string circuit.
<i>System fault string</i>	State of the system fault string circuit.

Function configuration

The following table specifies the *Hardware Fault Strings* configuration parameters.

Parameter	Description
<i>Inh sim Loc/Sys flt</i>	Disables the hardware fault string validation in simulation mode only.

Faults and alarms

The following table specifies the faults and alarms associated with the *Hardware Fault Strings*.

Fault/Alarm	Description
<i>Local flt</i>	Trip fault that occurs when the local fault string circuit is open.
<i>System flt</i>	Trip fault that occurs when the system fault string circuit is open.

Function description

The hardware fault string circuits are capable of operating with either 24 volts DC or 115 volts AC. The inputs are isolated so the system and local fault string circuits are not required to operate at the same voltage level. Both circuits must be closed for normal product operation.

The local fault string circuit is closed when the following connections are made through appropriate circuitry:

- Terminal board (ATBA): Connector L115 or L24 to connector LCOM.
- Backplane: Jumper J2 pin 1 to pin 2.

The system fault string circuit is closed when the following connection is made through appropriate circuitry:

- Terminal board (ATBA): Connector S115 or S24 to connector SCOM.

The local and system fault strings are evaluated by the hardware. If one of the strings opens during product operation, the hardware implements a controlled shutdown of the power bridge and dropout of the contactors.

The state of the hardware fault string inputs are reported to the control, and are contained in the variables *Local fault string* and *System fault string*. The variables contain the actual state of the hardware circuits, whether or not the product is running. The trip faults associated with the fault strings, *Local flt* and *System flt*, are reported when the fault string opens only when the product is running or commanded to run.

Heatsink Thermal Protection

The *Heatsink Thermal Protection* function measures the power bridge heatsink and ambient temperatures, and verifies that they are at a safe operating level.

Different bridge frame sizes require different sets of hardware thermal inputs, and generate different sets of temperature variables and faults. Click on one of the frame sizes below for more information on the *Heatsink Thermal Protection* function.

Frame sizes 375, 620

The *Heatsink Thermal Protection* function measures two power bridge heatsink temperatures and one ambient temperature for frame sizes 375 and 620.

Function inputs

The inputs to the *Heatsink Thermal Protection* function are hardware thermal sensor connections. The following table specifies the required thermal sensor connections to backplane connector J4.

<i>J4 pins</i>	<i>Required connection</i>
1 & 2	Heatsink A thermal sensor
3 & 4	Heatsink B thermal sensor
5 & 6	Open
7 & 8	Ambient thermal sensor

Function outputs

The following table specifies the output variables of the *Heatsink Thermal Protection* function.

<i>Variable</i>	<i>Description</i>
<i>Heat sink temp, A</i>	Measured heatsink A temperature. Degrees C or Degrees F
<i>Heat sink temp, B</i>	Measured heatsink B temperature. Degrees C or Degrees F
<i>Ambient temp</i>	Measured bridge ambient temperature. Degrees C or Degrees F

In simulator mode, the output variables are set to constant values; the maximum expected operating temperatures.

Related faults and alarms

The following faults and alarms are declared by the *Heatsink Thermal Protection* function.

- *HtSink over temp, A*
- *HtSink over temp, B*
- *Ambient over temp*
- *HtSink temp hot, A*
- *Htsink temp hot, B*
- *Ambient temp hot*
- *HtSink temp low, A*
- *HtSink temp low, B*
- *Ambient temp low*
- *HtSink sensor A bad*
- *HtSink sensor B bad*
- *HtSink rise high, A*
- *HtSink rise high, B*
- *HtSink temp imbalanc*
- *HtSink C miswired*

Frame sizes 1000, 1800

The *Heatsink Thermal Protection* function measures three power bridge heatsink temperatures and one ambient temperature for frame sizes 1000 and 1800.

Function inputs

The inputs to the *Heatsink Thermal Protection* function are hardware thermal sensor connections. The following table specifies the required thermal sensor connections to backplane connector J4.

<i>J4 pins</i>	<i>Required connection</i>
1 & 2	Heatsink A thermal sensor
3 & 4	Heatsink B thermal sensor
5 & 6	Heatsink C thermal sensor
7 & 8	Ambient thermal sensor

Function outputs

The following table specifies the output variables of the *Heatsink Thermal Protection* function.

<i>Variable</i>	<i>Description</i>
<i>Phase A HtSink temp</i>	Measured heatsink A temperature. Degrees C or Degrees F
<i>Phase B HtSink temp</i>	Measured heatsink B temperature. Degrees C or Degrees F

<i>Phase C HtSink temp</i>	Measured heatsink C temperature. Degrees C or Degrees F
<i>Ambient temp</i>	Measured bridge ambient temperature. Degrees C or Degrees F

In simulator mode, the output variables are set to constant values; the maximum expected operating temperatures.

Related faults and alarms

The following faults and alarms are declared by the *Heatsink Thermal Protection* function.

- *HtSink A over temp*
- *HtSink B over temp*
- *HtSink C over temp*
- *Ambient over temp*
- *HtSink A temp hot*
- *HtSink B temp hot*
- *HtSink C temp hot*
- *Ambient temp hot*
- *HtSink A temp low*
- *HtSink B temp low*
- *HtSink C temp low*
- *Ambient temp low*
- *HtSink A sensor bad*
- *HtSink B sensor bad*
- *HtSink C sensor bad*
- *HtSink A rise high*
- *HtSink B rise high*
- *HtSink C rise high*
- *HtSink temp imbalanc*

IGBT Thermal Protection

The *IGBT Thermal Protection* function implements a thermal model of the power bridge to determine the IGBT junction temperatures. It verifies the IGBTs are operating at a safe temperature.

Function inputs

The *IGBT Thermal Protection* function calculates the IGBT junction temperatures from the measured heatsink temperatures and phase currents.

The following table specifies the heatsink temperature variables according to bridge frame size.

Frame size	Heatsink temperature variables
375, 620	Heat sink temp, A, Heat sink temp, B

The following table specifies the phase current variables.

Variable	Description
Phase A current	Phase A current feedback. Amps
Phase B current	Phase B current feedback. Amps
Phase C current	Phase C current feedback. Amps

Function outputs

The following table specifies the output variables of the *IGBT Thermal Protection* function.

Variable	Description
Peak IGBT temp	Maximum IGBT junction temperature. Degrees C or Degrees F

Related faults and alarms

The following faults and alarms are declared by the *IGBT Thermal Protection* function.

- IGBT AL temp hot
- IGBT AU temp hot
- IGBT BL temp hot
- IGBT BU temp hot
- IGBT CL temp hot
- IGBT CU temp hot
- IGBT AL over temp
- IGBT AU over temp
- IGBT BL over temp
- IGBT BU over temp
- IGBT CL over temp
- IGBT CU over temp

Line-Line Voltage Protection

The drive contains several diagnostic and protective features involving the *Line-Line Voltage Protection*.

Function configuration

The following table specifies the *Line-Line Voltage Protection* configuration parameters.

Parameter	Description
Line OV fault lvl	AC line over-voltage trip threshold
Line OV alm on lvl	AC line over-voltage alarm on threshold

<i>Line OV alm off lvl</i>	AC line over-voltage alarm off threshold
<i>Line UV fault lvl</i>	AC line under-voltage trip threshold
<i>Line UV alm on lvl</i>	AC line under-voltage alarm on threshold
<i>Line UV alm off lvl</i>	AC line under-voltage alarm off threshold
<i>Over frq flt lvl</i>	AC line over-frequency trip threshold
<i>Over frq alm on lvl</i>	AC line over-frequency alarm on threshold
<i>Over frq alm off lvl</i>	AC line over-frequency alarm off threshold
<i>Low frq flt lvl</i>	AC line under-frequency trip threshold
<i>Low frq alm on lvl</i>	AC line under-frequency alarm on threshold
<i>Low frq alm off lvl</i>	AC line under-frequency alarm off threshold

Diagnostic variables

The following tables specifies the *Line-Line Voltage Protection* diagnostic variables.

Variable	Description
<i>Output volts, A-B</i>	Filtered A-B line-line voltage, volts
<i>Output volts, B-C</i>	Filtered B-C line-line voltage, volts
<i>A-B, Voltage offset</i>	Calculated A-B voltage offset, volts
<i>X-axis volt fbk</i>	X-component of ac line voltages - sampled at fast rate
<i>Y-axis volt fbk</i>	Y-component of ac line voltages – sampled at fast rate
<i>Vx, X-axis voltage</i>	Filtered version of <i>X-axis volt fbk</i>
<i>Vy, Y-axis voltage</i>	Filtered version of <i>Y-axis volt fbk</i>
<i>B-C, Voltage offset</i>	Calculated B-C voltage offset, volts
<i>Line monitor volt</i>	AC line voltage magnitude – filtered
<i>Line monitor frq</i>	AC line frequency – filtered
<i>Stopped</i>	The source is stopped
<i>PLL proven</i>	PLL is proven

Faults and alarms

The following table specifies the faults and alarms associated with the *Line-Line Voltage Protection*.

Fault/Alarm	Description
<i>A-B voltage offset</i>	Trip fault that occurs when the A-B line-line voltage offset is too high
<i>B-C voltage offset</i>	Trip fault that occurs when the B-C line-line voltage offset is too high
<i>AC line over voltage</i>	Trip fault that occurs when the line to line voltage magnitude is too high
<i>AC line voltage high</i>	Brief fault that occurs when the line to line voltage magnitude is too high and is approaching the trip

	level.
<i>AC line under volt</i>	Trip fault that occurs when the line to line voltage magnitude is too low.
<i>AC line volts low</i>	Brief fault that occurs when the line to line voltage magnitude is too low and is approaching the trip level.
<i>AC line over freq</i>	Trip fault that occurs when the calculated ac line frequency is too high
<i>AC line freq high</i>	Brief fault that occurs when the ac line frequency is too high and is approaching the trip level.

Function description

Voltage Offset Detection

The variables *Output volts, A-B* and *Output volts, B-C* are filtered versions of the measured line-line voltage feedbacks. The default filter frequency is 1000 rad/sec.

The source performs an automatic voltage offset calculation when running. Any appreciable offset voltage detected during the calculation indicates a potential power bridge or feedback circuitry problem. The *A-B voltage offset* and *B-C voltage offset* trip faults are reported when excessive offsets are calculated. The control uses the calculated offsets *A-B, Voltage offset* and *B-C, Voltage offset* to calculate feedbacks once the drive starts running. The control calculates the threshold for the offset faults.

The following faults are only active if *PLL proven* and *Stopped* are both true.

AC Line Overvoltage Detection

The regenerative source cannot operate effectively if the ac line voltage remains too high. This condition presents hazard to the power devices, as well as to the control algorithm. The *AC line voltage high* will indicate an over-voltage condition of the line when the filtered line magnitude, *Line monitor volt*, exceeds the user parameter, *Line OV alm on lvl*. This alarm will persist until *Line monitor volt* drops below the level, *Line OV alm off lvl*. If the voltage exceeds the level *Line OV fault lvl*, the source will trip with the fault, *AC line over voltage*. The settings for these user level parameters are calculated by the control during the commissioning exercise using the following rules:

Line OV alm on lvl = 112% of nominal ac line voltage

Line OV alm off lvl = 110% of nominal ac line voltage

Line OV fault lvl = 117% of nominal ac line voltage

AC Line Undervoltage Detection

The source will alarm and/or trip if the ac line magnitude dips too low. The alarm, *AC line volts low*, will indicate an under-voltage condition of the line when the filtered line magnitude, *Line monitor volt*, dips below the value of the user parameter, *Line UV alm on lvl*. This alarm will persist until *Line monitor volt* exceeds the level *Line UV alm off lvl*. If the voltage dips below the level *Line UV fault lvl*, the source will trip with the fault *AC line under volt*. The settings for these user level parameters are calculated by the control during the commissioning exercise using the following rules:

Line UV alm on lvl = 88% of nominal ac line voltage

Line UV alm off lvl = 90% of nominal ac line voltage

Line UV fault lvl = 50% of nominal ac line voltage

AC Line Overfrequency Detection

The source will alarm and/or trip if the ac line frequency is too high. The alarm, *AC line freq high* will indicate an over-frequency condition of the line when the filtered line magnitude, *Line monitor freq*, goes above the value of the user parameter, *Over freq alm on lvl*. This alarm will persist until *Line monitor freq* goes below the level, *Over freq alm off lvl*. If the frequency goes above the level *Over freq flt lvl*, the source will trip with the fault, *AC line over freq*. The settings for these user level parameters are calculated by the control during the commissioning exercise using the following rules:

Over freq alm on lvl = nominal frequency + 17.28rad/sec

Over freq alm off lvl = nominal frequency + 15.71rad/sec

Over freq flt lvl = 125% of nominal frequency

AC Line Underfrequency Detection

The source will alarm and/or trip if the ac line frequency is too low. The alarm, *AC line freq low* will indicate an under-frequency condition of the line when the filtered line magnitude, *Line monitor freq*, goes below the value of the user parameter, *Low freq alm on lvl*. This alarm will persist until *Line monitor freq* goes above the level, *Low freq alm off lvl*. If the frequency goes above the level *Low freq flt lvl*, the source will trip with the fault, *AC line under freq*. The settings for these user level parameters are calculated by the control during the commissioning exercise using the following rules:

Low freq alm on lvl = nominal frequency - 17.28rad/sec

Low freq alm off lvl = nominal frequency - 15.71rad/sec

Low freq flt lvl = 50% of nominal frequency

Phase Current Protection

The drive contains several diagnostic and protective features involving *Phase Current Protection*.

Diagnostic variables

The following tables specifies the *Phase Current Protection* diagnostic variables.

Variable	Description
<i>Phase A current</i>	Filtered phase A current, amps
<i>Phase B current</i>	Filtered phase B current, amps
<i>Phase C current</i>	Filtered phase C current, amps
<i>Phs A current offset</i>	Calculated phase A current offset, amps
<i>Phs B current offset</i>	Calculated phase B current offset, amps
<i>Phs C current offset</i>	Calculated phase C current offset, amps
<i>Ia^2 filtered</i>	Squared phase A current, RMS amps ²
<i>Ib^2 filtered</i>	Squared phase B current, RMS amps ²
<i>Ic^2 filtered</i>	Squared phase C current, RMS amps ²
<i>Real current fbk</i>	X-component of phase currents – sampled at

	fast rate
<i>Reactive current fbk</i>	Y-component of phase currents – sampled at fast rate
<i>Real pwr cur</i>	Filtered <i>Real current fbk</i>
<i>Reactive cur</i>	Filtered <i>Reactive current fbk</i>

Function configuration

The following table specifies the *Phase Current Protection* configuration parameters.

Parameter	Description
<i>Disable TOC profile</i>	Disables the application of the timed over current profile to the squared phase currents

Faults and alarms

The following table specifies the faults and alarms associated with the *Phase Current Protection*.

Fault/Alarm	Description
<i>Phase A cur offset</i>	Trip fault that occurs when the phase A current offset is too high
<i>Phase B cur offset</i>	Trip fault that occurs when the phase B current offset is too high
<i>Phase C cur offset</i>	Trip fault that occurs when the phase C current offset is too high
<i>Timed over current</i>	Trip fault that occurs when one of the squared phase currents is too high
<i>TOC pending</i>	Alarm that occurs when one of the squared phase currents is too high

Function description

The variables *Phase A current*, *Phase B current*, and *Phase C current* are filtered versions of the measured phase current feedbacks. The default filter frequency is 1000 rad/sec. These three signals are used for diagnostics only.

The source performs an automatic current offset calculation when it is stopped. During the calculation, the power bridge is turned off and the phase currents should be zero. Any appreciable phase current that is detected during the calculation indicates a potential power bridge or feedback circuitry problem. The *Phase A cur offset*, *Phase B cur offset*, and *Phase C cur offset* trip faults are reported when excessive offsets are calculated. The calculated offsets *Phs A current offset*, *Phs B current offset*, and *Phs C current offset* are used by the control to null the feedbacks once the drive starts running.

The source performs a timed over current (TOC) detection. The TOC detection filters the squared phase currents, applying a TOC cooling profile to the filter. The TOC cooling profile is turned off if parameter *Disable TOC profile* is set to *True* (the default value). If any of the squared phase currents is high enough to warrant caution, the *TOC pending* alarm is reported. If any of the squared phase currents is excessively high, the *Timed over current* trip fault is reported. The alarm and fault thresholds are calculated so the alarm occurs when the source exceeds its rated current and trips when it is applied at 150% of rated current for over 60 seconds.

DC Link Protection

The drive contains several diagnostic and protective features involving the *DC Link Protection*.

Diagnostic variables

The following tables specifies the *DC Link Protection* diagnostic variables.

Variable	Description
<i>DC bus feedback</i>	Unfiltered DC link voltage, DC volts
<i>DC voltage feedback</i>	FIR filtered <i>DC bus feedback</i> used for voltage regulator.
<i>AC line input power</i>	Filtered AC line power at source terminals
<i>DC bus current</i>	Filtered, estimated source dc current
<i>DC bus voltage</i>	Filtered DC link voltage, DC volts
<i>Running</i>	Indicates whether the source is ready to accept load and therefore whether the dc link voltage is within regulation.

Function configuration

All dc link protection settings are final values calculated by the control.

Faults and alarms

The following table specifies the faults and alarms associated with the *DC Link Protection*.

Fault/Alarm	Description
<i>DC bus over voltage</i>	Trip fault that occurs when the DC link voltage is too high
<i>DC bus under voltage</i>	Trip fault that occurs when the DC link voltage is too low

Function description

The signal *DC bus feedback* is an unfiltered representation of the DC link voltage. *DC bus voltage* is a filtered version of the DC link voltage. The default filter frequency is 90 rad/sec.

The *DC bus over voltage* trip fault occurs when the DC link voltage exceeds a maximum safe operating voltage defined as:

$$123\% \times \sqrt{2} \times \text{Max lineup output}.$$

The *DC bus under voltage* trip fault occurs when the drive is running and the DC link voltage falls below a minimum operating voltage. In both cases the minimum voltage is defined as:

$$50\% \times \sqrt{2} \times \text{Max lineup output}.$$

Max lineup output is specified during the drive commissioning process and should not be changed to alter the behavior of the DC link faults and alarms.

Transformer Overtemperature Detection

Those Innovation Series products that are part of a system containing a transformer can detect transformer overtemperature. The *Xfrmr over temp* trip fault and the *Xfrmr temp hot* alarm trigger on a signal that is a digital input from the transformer overtemperature fault circuit. Either the fault or alarm occurs when the transformer overtemperature circuit is open.

Function inputs

The following table specifies the input parameters of the *Transformer Overtemperature Detection* function.

Parameter	Description
<i>Xfrmr OT fault sel</i>	Selects the source of the transformer overtemperature circuit.

Function configuration

The following table specifies the configuration parameters of the *Transformer Overtemperature Detection* function.

Parameter	Description
<i>Xfrmr OT fault mode</i>	Specifies whether the overtemperature condition triggers a fault or an alarm.

Faults and alarms

The following table specifies the faults and alarms that the *Transformer Overtemperature Detection* function declares.

Fault/Alarm	Description
<i>Xfrmr over temp</i>	Occurs when the state of the transformer overtemperature circuit is <i>False</i> , indicating that the circuit is open, and parameter <i>Xfrmr OT fault mode</i> is set to <i>Trip flt</i> .
<i>Xfrmr temp hot</i>	Occurs when the state of the transformer overtemperature circuit is <i>False</i> , indicating that the circuit is open, and parameter <i>Xfrmr OT fault mode</i> is set to <i>Alarm fault</i> .

Function description

The parameter *Xfrmr OT fault sel* generally selects digital inputs (*Digital input 1*, ..., *Digital input 6*). The *Transformer Overtemperature Detection* may be disabled by setting *Xfrmr OT fault sel* equal to **Unused**.

Line Protection Module

The LPPA is the line protection module. This is an optional hardware module used by the source to determine ground faults. Source firmware reads two inputs from the LPPA to determine the presence of ground faults and the status of the MOV fuse. Those using this function should refer to the LPPA manuals for proper application and scaling information.

The ground fault detection portion of this protective is a pointer, *LPP gnd signal sel*, normally aimed at one of the configurable analog inputs, *Analog input 1 unfil*(default). This is a voltage signal representing ground fault current, but the default configuration for this protection function leaves the signal in volts and sets the alarm and trip thresholds as a voltage. A low pass filter is applied to the scaled input signal and the output of the filter, *LPPA gnd cur*, is tested against thresholds that are described below. If *LPPA gnd cur* rises above *LPPA gnd flt alm*, the alarm, *Ground flt alm, LP* will be given. If it falls back below *LPPA gnd flt clr*, the alarm will cease after the source has stopped. If the signal surpasses *LPPA gnd flt lvl*, the source will trip with (<<Lp_Gnd_Trip)>>.

The MOV fuse part of this function uses a pointer input, *LPP fuse blown sel*. As a default, this pointer is directed to *Digital input 2*. A low pass filter is applied to each digital input. Once read in the fuse, sense signal becomes *LPPA fuse stat*. If it is False, the alarm, *AC filter fuse blown*, will be given. The alarm will only clear if *LPPA fuse stat* becomes True again (by replacing the fuse).

The following tables show the parameters and variables for this function.

Parameter	Description
<i>LPP gnd signal sel</i>	LPPA ground fault signal pointer
<i>LPPA gnd flt scl</i>	Voltage to current scale factor which is applied to the input analog signal. This parameter is set to 1.0 as default, leaving the scaled signal output as a voltage.
<i>LPPA gnd flt fil</i>	The bandwidth of the low pass filter (rad/sec) applied to the analog input signal The default is set to the reciprocal of the execution rate of task2.
<i>LPPA gnd flt alm</i>	The level at which the alarm, <i>Ground flt alm, LP</i> , is set.
<i>LPPA gnd flt clr</i>	The level at which the alarm, <i>Ground flt alm, LP</i> , is cleared.
<i>LPPA gnd flt lvl</i>	The level at which the trip f
<i>LPP fuse blown sel</i>	LPPA MOV fuse sense signal pointer
<i>LPPA mode</i>	LPPA Absent/Present selection –populated during commissioning.
Variable	Description
<i>LPPA gnd cur</i>	Ground current indication (filtered). Note that this value may actually be scaled as the voltage sensed from the LPPA, not a current. If <i>LPPA gnd flt scl</i> is 1.0, this is the sensed voltage.
<i>LPPA gnd warning</i>	This variable is for external use to indicate that the alarm, <i>Ground flt alm, LP</i> is present.
<i>LPPA gnd trip</i>	This variable is for external use to indicate that the fault, <i>LPPA gnd trip</i> is present.
<i>LPPA fuse stat</i>	This signal, when True, indicates that the MOV fuse is ok When <i>LPPA mode</i> indicates that the LPPA module is not present, this variable will always be True.

Phase Imbalance Function

The source phase imbalance function is responsible for monitoring the condition of the phase imbalance on the ac line, as well as the status of the phase lock loop. Pertinent variables and are listed below.

Variables	Description
<i>Y axis line voltage</i>	The demodulated, y-component of the ac line voltage: the component that phase lock loops regulates to zero.
<i>PLL error</i>	This is the error signal of the phase lock loop.
<i>X axis line voltage</i>	The demodulated, x-component of the ac line voltage.
<i>Ac line magnitude</i>	This is the magnitude of <i>X axis line voltage</i> and <i>Y axis line voltage</i> (square root of squared sums). It represents the magnitude of the ac line.
<i>Phase imbalance sqr</i>	This signal is basic in the determination of phase imbalance, or phase lock loop goodness, for the source. It is the filtered sum of two squared signals. The first is <i>PLL error</i> , and the second is the difference between <i>X axis line voltage</i> and <i>Ac line magnitude</i> .
<i>Phase imbalance ref</i>	This signal represents the allowed amount of imbalance for the source. It has units of volts squared. It includes an allowance for noise and is compensated by the magnitude of the ac line.
<i>Phase imbalance avg</i>	This signal is the amount by which <i>Phase imbalance sqr</i> exceeds the allowed threshold, <i>Phase imbalance ref</i> .
<i>Phase imbalance int</i>	When <i>Phase imbalance avg</i> is greater than zero, it accumulates with dt compensation into this integrator. If the integrator exceeds the a clamp threshold, <i>Phs imbalance limit</i> , an alarm, <i>AC line transient</i> , will occur. If this condition persists for <i>Phs imbalance time</i> , the trip fault, <i>AC line watchdog</i> , will occur.
<i>Phs imbalance limit</i>	This is the clamp for <i>Phase imbalance int</i> . When <i>Phase imbalance int</i> is in this clamp, the alarm, <i>AC line transient</i> , will occur. If this condition persists for <i>Phs imbalance time</i> , the trip fault, <i>AC line watchdog</i> , will occur.
<i>PLL proven</i>	This Boolean indicates the status of the phase lock loop. It is directly effected by the phase imbalance detection circuit. When the ac line appears to the control after charging begins, there will a significant, transient error until the loop locks. <i>Phase imbalance avg</i> will thus be significant, but will begin to decay as the loop locks. After <i>Phase imbalance int</i> is less than zero for about 120 msec, <i>PLL proven</i> will be set true and the phase lock loop will be declared

ready for use. In order for *PLL proven* to be set False after it is set True, *AC line loss* must be true for 1sec. or *Phase imbalance int* must be non-zero for 1sec.

AC line loss

If the ac line drops below 10% of nominal for 5 msec, *AC line loss* will be set True, declaring that the ac line has been lost. This will immediately cause the *AC line transient* alarm. If the condition persists for 1second, the source will trip if it has not already. *AC line loss* will be set False again as soon as the ac line rises back above 15% of nominal.

The **Ovr_Line_Mon** diagram, as seen through the toolbox, shows a one line of the phase imbalance scheme.

Sequencer Functions

Sequencer Overview

Sequencing is a key function of the Innovation Series source. The sequencer oversees the starting and stopping of the source. It protects from the mis-operation of the source during fault or diagnostic conditions. The sequencer also provides source status information that can be used by various source and application functions.

The Innovation Series source sequencer can be described by the following functions:

- *Fault Reset Logic*
- *Sequencer Permissives*
- *Stopping Commands*
- *Sequencer Commands*
- *Sequencer Status*
- *Contactor Commands and Feedbacks*

Fault Reset Logic

The sequencer oversees the shutdown of a source under a fault condition. It insures that the contactors are opened and the regulators are disabled in a timely manner.

Faults can be reset in several different ways. They can be reset from the source DDI, by a selected variable, or through the LAN, if enabled.

Function inputs

<i>Parameter</i>	<i>Description</i>
<i>Fault reset select</i>	Specifies a Boolean variable that requests a fault reset, when the variable transitions from a 0 to a 1 (Positive edge detected).
<i>Variable</i>	<i>Description</i>
<i>Fault reset req, lan</i>	Requests a fault reset when the LAN is active and

variable transitions from a 0 to a 1 (positive edge detected). Refer to *LAN Signal Map*. This variable must be selected in *Fault reset select* to be active.

**DDI “Reset Faults”
Push Button** Requests a fault reset when pressed.

Function outputs

<i>Variable</i>	<i>Description</i>
<i>Trip fault active</i>	Indicates when a trip fault is present. <i>Trip fault active</i> is True when a trip fault exists. It is a NC contact in the <i>Ready to run</i> permissive string. Refer to <i>Sequencer Permissives</i> .
<i>No trip fault</i>	Indicates when a trip fault is NOT present. Is True when there is no trip fault. (Alarm may exist).
<i>No faults active</i>	Indicates when no trip faults or Alarms are present. Is True when no faults or alarms exist in the source.

Function description

When the source is running and a trip fault is generated, the sequencer will perform the following actions in order:

- Disables the bridge power enable, *Bridge is on*.
- Disables the voltage and current regulators via *Inner reg enable*.
- Commands the main contactor to open via *MA close command*

The sequencer also removes any type of run request to the source because the *Ready to run* permissive string drops out due to the trip fault. This will also prevent the source from trying to run while a trip fault is present.

When a trip fault occurs, the bridge is turned off quickly without a ramp down of any kind. The source cannot control the loading on the dc link.

To reset a trip fault or alarm, request a fault reset using one of the Function inputs described above.

Note: Performing a fault reset may not clear the fault if the condition still exists, or if the fault is locked.

Sequencer Permissives

Sequencer permissives are used to prevent or allow the source to run if the permissive condition exists in the source. There are two types of permissives: internal permissives and application permissives.

Internal permissives are internal source conditions that must be satisfied before the source will run. The current offsets must be valid, that is, the offset calculation must have run for 1.0 second after power-up or after a stop.

Application permissives allow the user to connect application specific permissive logic that must be satisfied before the source will run.

The main permissive string used by the sequencer is *Ready to run*. This permissive must be *True* for the source to run and the details of this permissive are displayed in the Sequencing diagrams in the source.

Function inputs

Application Permissive Inputs

<i>Variable</i>	<i>Description</i>
<i>X stop active</i>	If <i>True</i> , this permissive will prevent the source from starting or will perform an X-Stop if the source is running.

Internal Permissive Inputs

<i>Variable</i>	<i>Description</i>
<i>Local fault string</i>	Local hardware permissive. When <i>Local fault string</i> is <i>True</i> , it will prevent the source from starting or running. If a run is requested while <i>Local fault string</i> is <i>True</i> , a trip fault, <i>Local flt</i> , will be generated.
<i>System fault string</i>	System hardware permissive. When <i>System fault string</i> is <i>True</i> , it will prevent the source from starting or running. If a run is requested while <i>System fault string</i> is <i>True</i> a trip fault, <i>System flt</i> , will be generated. See also <i>Hardware Fault Strings</i> .
<<(Crwbr_Rdy)>>	Indicates the crowbar resistors are thermally ready after a crowbar firing.

Function outputs

<i>Variable</i>	<i>Description</i>
<i>Ready to run</i>	The main run permissive and primary indication that the source is ready to run. If <i>False</i> , this permissive will cause all run requests and commands to drop out. The source cannot be started unless <i>Ready to run</i> is <i>True</i> .

Related faults and alarms

The following faults and alarms may be generated when the *Ready to run* permissive is not satisfied.

- *Local flt*
- *System flt*

Related functions

- <<(CrwbrFunc)>>

Stopping Commands

The sequencer provides two mechanisms for issuing a controlled stop of the source: a Normal stop and an X-stop.

A Normal stop can be issued in several ways:

- Removing a run request
- Pressing the Stop pushbutton on the DDI (also called the keypad),

- Causing a downward transition to the variable or input to which *Hardware run ptr* is pointed.

An X-Stop is issued only through ISBus for the source. The stop mechanism is no different than the others for the case of the source.

A third mechanism for stopping the source is to generate a trip fault. In this case, the shutdown is essentially the same as the others described here.

Normal stop

The Normal stop is the typical way to stop the source in a controlled manner. A Normal stop can be configured as Ramp stop, Coast stop, or Quick stop.

Function inputs

The following parameters source the function input variables:

<i>Parameter</i>	<i>Description</i>
<i>Hardware run ptr</i>	See <i>Sequencer Commands</i> for a description of this parameter.

The following variables are inputs that are used to stop the source.

<i>Variable</i>	<i>Description</i>
<i>Run request</i>	A normal stop is generated when <i>Run request</i> is false.
DDI Stop Pushbutton	A normal stop is generated when the Stop pushbutton is pressed on the DDI.

X-Stop

The X-stop is an alternate way to stop the source in a controlled manner. An X-stop can only be issued via ISBus for the source.

Function inputs

<i>Variable</i>	<i>Description</i>
<i>X stop request, lan</i>	Is used to source <i>X stop active</i> from the LAN when <i>LAN commands OK</i> is True.

Once the source is stopped, *X stop active* must be set False before the source is re-started.

Sequencer Commands

A sequencer **request** is generated from various user inputs to direct the sequencer to either run. A sequencer command is the internal “go ahead” to sequencer once the permissive logic has been satisfied (see *Sequencer Permissives*).

The variable *Run request* is associated with Run Commands and direct the sequencer to run the source

Run Commands

A run command (initiated by *Run request*) will:

- Enable bridge power
- Cause the dc link to charge by closing the MB contactor

- After appropriate timing and the link is charged, command the MA contactor to close and open the MB contactor.
- Verify that the pll is locked
- Begin controlling link voltage by ramping the dc link reference.

Function inputs

Parameter	Description
<i>Hardware run ptr</i>	Selects an external input that can source <i>Run request</i> . This input is active in both “Remote mode” and “Local Mode”. This pointer was designed to point to one of the digital inputs. The sequencer behavior enables an automatic run request to be generated to the source after a power-up reset if the input to which <i>Hardware run ptr</i> is pointed is high. After power-up, this signal is transition detected. A low to high transition will attempt to issue a run command and a high to low transition will stop the source if it is running.

Variable	Description
<i>Hardware run request</i>	Sets/clears <i>Run request</i> when <i>Hardware run ptr</i> is used
DDI Run pushbutton	Sets <i>Run request</i> to True if the source is in Local mode (<i>Local mode active</i> is True).

Function outputs

Variable	Description
<i>Run request</i>	The request to run the source. The details of the logic which forms this signal is shown in the sequencer diagrams.
<i>Run command</i>	Internal sequencer command formed from <i>Run request</i> , and the <i>Ready to run</i> permissive string.

Sequencer Status

The sequencer provides source status information that can be used by various application functions and is also used for internal sequencing functions. The status information is divided into two types:

- source status variables
- Sequencer status variables

Source status variables

Source status variables provide general information about the status of the source (e.g. whether it is running, stopped, etc.) These variables are used by the toolbox and DDI to provide source status information to the user. Source status information is provided to the LAN as well. (See *LAN Signal Map*.)

Variable	Description
<i>Bridge is on</i>	Bridge power is enabled.

<i>No faults active</i>	No faults or alarms exist in the source.
<i>Ready to run</i>	The source is ready to run and will start if a run is requested. (See <i>Sequencer Permissives</i> .)
<i>Running</i>	The source is running (i.e. the regulators are enabled).
<i>Stopped</i>	The source is stopped (i.e. bridge power is off).
<i>Trip fault active</i>	A trip fault exists in the source.
<i>Link charging</i>	The source is charging the link. The variable, <i>DC link charging</i> , is set when the link is charging and the charge resistor thermal model is active.

Source request variables

Sequencer status variables are used to request and report status of internal regulator sequencing. These variables normally come in pairs of a **Request** and a **Status**. The **Request** is a command to either enable or disable the appropriate function. The **Status** is a feedback that indicates the command has been successfully executed (i.e. enabled or disabled) and the sequencer can proceed to its next state.

Variable	Description
<i>Sequencer state</i>	Internal sequencer state variable that indicates what mode the sequencer is in. Possible values include: • Stopped • Charge • PLL sync • Running • Diagnostic mode
<i>Charge enable state</i>	Indicates that the link charge task is complete. The link is charged
<i>Seq sync request</i>	Request to check that the pll is proven <i>PLL proven</i> .
<i>Seq sync status</i>	The pll was seen proven when checked.
<i>Reg enable request</i>	Request to enable (disable) all regulators.
<i>Reg enable status</i>	Status that all regulators are enabled (disabled).
<i>Charge enable req</i>	Request to charge the link. The associated task will manipulate the charge contactor (MB) and main contactor(MA) in order to accomplish the requested task.

Contactor Commands and Feedbacks

The sequencer normally controls the operation of the main (MA) contactor and the charge contactor(MB). The source sequencer controls these two contactors in charging the link and then in preparing the source to run.

When the source is commanded to run, the sequencer commands the charge contactor to close. This allows the dc link to charge as current charges the capacitors through the charge resistors.

When the link voltage reaches apx. 80% of nominal voltage, the sequencer closes the main contactor and shortly thereafter opens the charge contactor. This allows the link to charge in a controlled manner and then allows the charge resistor to be

removed from the circuit so that the operating current can flow through the main contactor. The table below lists the three primary contactor command/status variables.

<i>Variable</i>	<i>Description</i>
<i>MA close command</i>	Sequencer command to close the main contactor
<i>MA contactor closed</i>	Feedback to the control that tells the status of the main contactor(open or closed).
<i>Charge cont command</i>	Sequencer command to close the charge contactor

Source Configuration Functions

Intelligent Part Number (IPN)

The Intelligent Part Number (IPN) specifies the Innovation Series product and the basic configuration of the product. The IPN is the catalog number for the Innovation Series product. It can be found on the inside of the cabinet door.

The IPN for the Innovation Series regenerative source with general application pattern takes the following form:

ACCBR-A-FRAM-VOLT-T-V-xxx-xxxx-x

The IPN contains eight fields separated by dashes. The fields shown in italics are user configurable.

Product field

The product field is designated by the characters ACCBR. The characters have the following meaning:

AC	AC line input
CB	Common bus
R	Regenerative

Pattern field

The pattern field is designated by the character A. The character has the following meaning:

A	General application firmware pattern
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Frame size field

The frame size field is designated by the characters *FRAM*. The designation has the following meaning:

<i>FRAM</i>	Bridge frame size
-------------	-------------------

The following regenerative source frame sizes are supported:

0375, 0620, 1000, 1800

System voltage field

The system voltage field is designated by the characters *VOLT*. The designation has the following meaning:

<i>VOLT</i>	Maximum lineup output AC voltage
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The regenerative source supports the following system voltages:

0575

Total harmonic distortion (THD) field

The THD is designated by the character *T*. The designation has the following meaning:

T Total harmonic distortion (THD) selection

The THD selection determines the shunt rating, reactor characteristics, and chopping frequency. The regenerative source supports the following THD selections:

THD selection	Shunt ratings
A, Stnd/Rmot reactor	Standard selection. Normal THD (~15%). Remote reactor.
B, Prem/Rmot reactor	Premium selection. Low THD (<15%). Remote reactor.

Bridge Version field (Vers) field

The version is designated by the character *V*. The designation has the following meaning:

V Bridge version

The bridge version selection must correspond with the nameplate version number of the bridge. This is critical. Bridge version changes when a bridge component changes. This affects configuration of the control. Failure to select the correct bridge version can prevent proper operation of the source, disable needed protections, or cause feedback mis-scalings.

Primary Source & Application Data

User entered parameters

Several primary values define the ac line characteristics for the Innovation Series general industrial application (GIA) pattern regenerative source. The primary values include ac line frequency and voltage

The primary values are used to determine control and protective settings for the drive.

The following table lists the user entered parameters that specify the primary data:

Parameter	Description
<i>AC input voltage</i>	AC line voltage (rms) at bridge terminals
<i>Input frequency</i>	AC line frequency
<i>Max lineup output</i>	Maximum drive output voltage – determines dc link setpoint.
<i>Phase rotation req</i>	Ac line phase sequence rotation request

This product is designed to require very few user inputs. It essentially acts a power supply, and is expected to provide a stable and dependable dc link with very little user information. Many calculated final values are derived from these few user inputs.

Display meter scaling parameters

The Innovation Series Regenerative Source contains a set of parameters, which specify the scaling for the DDI and toolbox display meters. These parameters are calculated from the primary motor and application parameters. They are calculated within either the *Source Commissioning* wizard or the *Per Unit Setup* wizard. If any of the primary data parameters is modified outside the *Source Commissioning*

wizard, the *Per Unit Setup* wizard should be performed to update the display meter scaling parameters.

Source Control Functions

Inner Current Regulator

The Current Regulator implements the dc link voltage regulator and reactive current regulator commands. It provides proportional and integral (P-I) structure for each command, separately in the x-y vector axes. The proportional path provides quick response, while the integral path forces the feedbacks to match the commands in steady state. The integrators do not windup if subsequent limits prevent regulation.

Additional features include:

- A phase imbalance compensator, which within a limited range effectively prevents the converter from outputting unbalanced currents even in the presence of unbalanced input voltages.
- X-axis spillover, which allows continued regulation of both real power current and dc bus voltage if the ac input voltage exceeds the maximum attainable by pwm modulation of the present dc bus voltage (such as during an ac line overvoltage condition or a severe impact load on the dc bus). Sustained regulation is achieved by increasing reactive current flow through the external inductances, which lowers the ac voltage at the source's bridge terminals.
- Command conditioning blocks, which model the system response to changes in current command, and provide two outputs. The first is a voltage feed forward, which is the current command multiplied by system impedance. The other output, provided to the regulator's integrator, filters the input current command to help prevent integrator windup during the delayed feedback response to fast changes. The current conditioning blocks allow strong proportional and feed forward gains for optimized regulator response.
- Prior to pwm startup the current regulator is set to match the incoming line voltage. Upon startup nominal voltage is used (see parameter descriptions below).

The outputs of the Current Regulator go on to the PWM modulator to be turned into the desired power device on/off gate signals that will cause the desired current response (hence desired dc voltage and reactive current response).

Two adjustable parameters are provided, but in virtually all applications they do not need to be changed. They are automatically set to defaults by the source commissioning procedure. They are:

- *AC input voltage* - provides the steady state bias to the x-axis current regulator, in effect setting the nominal ac side voltage of the PWM source equal to nominal ac line voltage.
- *Ix reg w dfwd* - This startup bias filter softens the change in bias upon pwm startup. It has no effect in steady state.

The gains of the inner current regulator are final values, and are not intended to be modified by the user. The gains are calculated as functions of the few user input parameters in the commissioning wizard. However, these gains are shown here for user convenience as "read-only" vars. The tables below show each of the gains and the signals in the regulator on a channel by channel basis.

X-channel regulator gains and limits

The following table specifies the *Inner Current Regulator* X-channel current regulator gains and limits.

Variable	Description
<i>Ix reg command gain</i>	X-channel proportional command gain
<i>Ix reg feedback gain</i>	X-channel proportional feedback gain
<i>Ix reg integral gain</i>	X-channel integral gain
<i>Ix reg int limit</i>	X-channel integral limit
<i>Ix reg U/D limit</i>	X-channel modulation limit
<i>Ireg spillover gain</i>	X-channel spill-over gain

X-channel regulator signals

The following tables specifies the *Inner Current Regulator* X-channel current regulator signals

Variable	Description
<i>Real cur command</i>	X-channel current regulator command from voltage regulator
<i>Ix command delayed</i>	X-channel delayed current command
<i>Ireg X volt fdfwd</i>	X-channel command voltage feed-forward
<i>Ireg X integral term</i>	X-channel current regulator integrator
<i>Ireg voltage fdfwd</i>	X-channel nominal voltage feed-forward
<i>Ix reg error</i>	X-channel current error for integral path
<i>Ix reg spillover</i>	X-channel current spill-over into Y channel
<i>Ix U/D in neg lim</i>	X-channel current regulator output in negative limit
<i>Ix U/D in pos lim</i>	X-channel current regulator output in positive limit
<i>Ireg voltage fdfwd</i>	X-channel nominal line voltage feed-forward
<i>Nominal input volts</i>	Nominal line to neutral input voltage
<i>DC volts reciprocal</i>	Reciprocal of dc link voltage for construction of modulation cmd
<i>Ireg X U/D</i>	X-channel up/down command prior to phase imbalance adjustment
<i>X axis modulation</i>	X-channel current regulator output modulation command
<i>Ix reg phs imb comp</i>	X-channel current regulator output voltage command
<i>Ix reg voltage out</i>	X-channel current regulator output voltage command

Y-Channel regulator gains and limits

The following tables specifies the *Inner Current Regulator* X-channel current regulator gains and limits.

Variable	Description
<i>Iy reg cmd limit</i>	Y-channel inner regulator current command clamp

<i>Iy reg cmd gain</i>	Y-channel proportional command gain
<i>Iy reg fbk gain</i>	Y-channel proportional feedback gain
<i>Iy reg int gain</i>	Y-channel integral gain
<i>Iy reg int limit</i>	Y-channel integral limit
<i>Iy reg U/D limit</i>	Y-channel up/down limit

Y-channel regulator signals

The following tables specifies the *Inner Current Regulator* X-channel current regulator signals

Variable	Description
<i>Internal Iy fbk</i>	Y-channel current regulator command from outer reactive current regulator
<i>Iy reg ind V dfwd</i>	Y-channel current regulator voltage feed-forward
<i>Reactive cur command</i>	Y-channel current regulator command from outer reactive current regulator, clamped with spillover from x-channel added.
<i>Iy command delayed</i>	Y-channel delayed current command
<i>Iy reg error</i>	Y-channel current error for integral path
<i>Ireg Y integral term</i>	Y-channel current regulator integrator
<i>Iy U/D in neg lim</i>	Y-channel current regulator output in negative limit
<i>Iy U/D in pos lim</i>	Y-channel current regulator output in positive limit
<i>Nominal input volts</i>	Nominal line to neutral input voltage
<i>Ireg Y U/D</i>	Y-channel modulation command prior to phase imbalance adjustment
<i>Ireg Y volt dfwd</i>	Y-channel voltage feed-forward($I_x \cdot W \cdot L$)
<i>Y axis modulation</i>	Y-channel current regulator output modulation command
<i>Iy reg phs imb comp</i>	Y-channel current regulator output voltage command
<i>Iy reg volts out</i>	Y-channel current regulator output voltage command
<i>Iy lim pos flag</i>	Y-channel input current in positive limit
<i>Iy lim neg flag</i>	Y-channel input current in negative limit

PWM Source Overview

The PWM source is a fully regenerative AC < -- > DC converter connected to the customer power grid, typically used to provide a symmetrical dc power source for multiple DC-Fed drives. In most standard applications the PWM source is configured to run at near unity power factor. It generates less ac line current distortion than standard rectifier sources. It can run through temporary ac system voltage dips with no disturbance to the drives, as long as its overload current rating is not exceeded. The PWM source can also provide Var support to the local grid, with

or without drives connected. With drives connected, reactive support is limited by the real power drawn by the drives.

The PWM source is comprised of the same power bridge and controller hardware as the dc fed drive of the same rating. Differences include startup charge control circuitry on the ac side and controller firmware. The PWM source requires series inductors and/or a transformer on the ac side.

For all applications, the PWM source's basic control strategy is to tightly maintain and regulate dc link voltage. The Vdc regulator implements its commands through a fast inner ac current regulator. An application Var or reactive current regulator can be overlaid on top of the Vdc regulator. A basic reactive current regulator is provided in the standard firmware.

Standard Innovation Series product protectives, diagnostic features, and interfaces to higher level control / monitoring are provided. Additional information is provided on other help screens.

Reactive Current Reference

The Innovation Series Regenerative IGBT source is capable of supplying reactive current to the incoming AC line, both when used as a regenerative source to AC drives or as a stand alone reactive VAR compensator. In either case, the primary use is to supply leading reactive volt-amperes (VARs) to the incoming supply to compensate for other connected loads lagging VARs and thereby correct the power factor of the overall system load to near unity (1.0) power factor. The lagging VARs are typically generated by other loads on the system such as auxiliary induction motors, lighting, or DC drives.

The Innovation Series regenerative source contains an imbedded PI type regulator, which will accept both an external reference and an external feedback to form an output error signal, which serves as a reference for the reactive current regulator of the source. This embedded regulator is designed to regulate total reactive VARs at an upstream point in the supply system using a remote sensor as feedback, or by setting the integral and feedback gains to zero. It can also serve as a straight in reference to set a fixed or dynamic level of reactive VAR output from the source using its own internal feedback.

Function inputs

The following table specifies the input parameters to the *Reactive Current Reference* function.

<i>Parameter</i>	<i>Description</i>
<i>Iy reference select</i>	Reactive current reference input. This reference can be from an external source through one of the A/D converter, or LAN variable from an ACL or PLC. It could also be one of the fixed preset references available within the MCL logic. In either case it is the variable which sets the reference for the amount of reactive current requested of the source.
<i>Iy feedback select</i>	Reactive current feedback input. This feedback signal is normally generated by an external sensor of reactive current via one of the A/D converter inputs or LAN variable from an ACL or PLC. This input is optional. (See modes of operation below).

The following table specifies the input variables to the *Reactive Current Reference* function.

Variable	Description
<i>Ix cmd avg</i>	<i>Ix</i> current command. This signal represents the real power to the DC bus when drives are connected to the source. It is used to limit the <i>Iy</i> output in cases where the source would be overloaded by the combination of the reactive current reference and the real power demand from the drives. In the case of no drives connected to the source, this signal remains essentially at 0 and has no effect.

The following table specifies the internal variables to the *Reactive Current Reference* function.

Variable	Description
<i>Iy ref limit max</i>	The dynamic maximum upper limit for the output of the <i>Reactive Current Reference</i> . If this product is a supplier to drives, this limit adjusts according to the reserve current capability of the source. If this product does not supply drives, the limit is set equal to <i>Iy ref max limit</i>
<i>Iy ref limit min</i>	The dynamic maximum lower limit for the output of the <i>Reactive Current Reference</i> . If this product is a supplier to drives, this limit adjusts according to the reserve current capability of the source. If this product does not supply drives, the limit is set equal to <i>Iy ref max limit</i> .
<i>Iy ref neg freeze</i>	This flag, when True, is used to prevent the integrator of the <i>Reactive Current Reference</i> from becoming more positive. It is set True when any of the following are true: <i>Iy lim pos flag</i> , <i>Ix U/D in neg lim</i> , or <i>Iy U/D in pos lim</i>
<i>Iy ref pos freeze</i>	This flag, when True, is used to prevent the integrator of the <i>Reactive Current Reference</i> from becoming more negative. It is set True when any of the following are true: <i>Iy lim neg flag</i> , <i>Ix U/D in pos lim</i> , or <i>Iy U/D in neg lim</i>
<i>Iy reference command</i>	The net command reference for the <i>Reactive Current Reference</i> . This is normally a current command. It is the value of command that has slew rate implemented.
<i>Iy reference error</i>	The error signal of the <i>Reactive Current Reference</i> .
<i>Iy reference fbk</i>	The feedback signal of the <i>Reactive Current Reference</i> . This signal is the scaled version of the signal pointed to by <i>Iy feedback select</i> .
<i>Iy reference limit</i>	Filtered value of <i>Reserve current</i> . It is filtered to soften the effect on the output limit. The response of the filter is determined by <i>Iy limit response</i> .
<i>Reserve current</i>	The calculated reactive current reserve as determined by a magnitude calculation, which considers the maximum allowed reactive current and the amount of real current presently used. This dynamically limits the reactive current to protect the source bridge and also to allow as much reactive current as possible when the source is lightly loaded from drives.

Function outputs

The following table specifies the output variables of the *Reactive Current Reference* function.

Variable	Description
<i>Internal Iy fbk</i>	Reactive current command to the Iy core control of the source controller. This signal sets the actual level of reactive current at the source input.
<i>Avg line voltage mag</i>	This input is used as a feedback, pointed to by <i>Iy feedback select</i> when in the voltage regulation mode.

Function configuration

The following table specifies the configuration parameters of the *Reactive Current Reference* function.

Parameter	Description
<i>Iy ref command scale</i>	Reference command scale. Scales the input reference command.
<i>Iy ref fbk scale</i>	Feedback scale. Scales the external feedback signal to the internal PI regulator.
<i>Iy reference adjust</i>	Reference command offset. Sets a fixed offset, which adds to the reference command.
<i>Iy ref current setpt</i>	Reference command setpoint. May be used as a fixed VAR reference command (in lieu of an external reference).
<i>Iy reference select</i>	Input reference command address. Selects which of several possible variable or setpoints to use as the reference command input.
<i>Iy feedback select</i>	External feedback address. Selects which of several possible variables contains the feedback signal for the PI regulator. Possible selections are: <i>Internal Iy fbk</i> , <i>Avg line voltage mag</i> , <i>LAN Iy fbk</i> , and <i>Analog input 2</i> . Selection depends upon the mode of operation.
<i>Iy slew rate</i>	Input reference command slew limit. Sets the maximum slew or ramp rate of the input reference command.
<i>Iy ref command gain</i>	Reference command regulator gain. Sets the reference gain command for the PI regulator.
<i>Iy ref int gain</i>	PI regulator integral gain. Sets the integral gain of the PI regulator.
<i>Iy ref loop gain</i>	External feedback regulator gain. Sets the feedback gain for the PI regulator.
<i>Iy ref int neg limit</i>	Integrator negative limit. Limits the PI regulator integrator output to prevent wind-up.
<i>Iy ref int pos limit</i>	Integrator positive limit. Limits the PI regulator integrator output to prevent wind-up.
<i>Max cur mag allowed</i>	Maximum reactive current limit setting. Sets maximum total current level above which Iy will be limited (below the reference command). This limit is set to protect the source from exceeding its RMS

	current rating.
<i>Iy limit response</i>	Reactive current limit filter. Sets the maximum response of the reactive current limit (to changes caused by varying Ix levels).
<i>Iy ref min limit</i>	Fixed minimum reactive current limit. Minimum limit on the reactive current reference command when source is used as a reactive VAR compensator (no drives attached).
<i>Iy ref volt setpt</i>	When the source runs in ac line voltage regulation mode, this parameter is the setpoint.
<i>Volt reduct mode</i>	This parameter is used only in the ac line voltage regulation mode. When set True, the source control will allow the ac voltage at the terminals of the source to reduce in order to accomplish voltage regulation.
<i>Iy ref max limit</i>	Fixed maximum reactive current limit. Maximum limit on the reactive current reference command when source is used as a reactive VAR compensator (no drives attached).

Functional Description

The reactive current regulator function provides a full PI regulator for use as a reactive power compensator and regulator for the AC power source. If properly sized, it can compensate the drive system reactive power to result in an overall average power factor of .99 +, which can greatly reduce the KVA demand of the system. The result is higher system efficiency and virtual elimination of power supply demand charges based on low power factor. It can also be used to supply reactive VAR compensation for other loads (outside the system) to raise the overall power factor at the substation level.

Several different modes of operation are possible with this system depending on how it is configured. The four most common modes of operation are described below, but others are also possible, as are combinations of the four modes.

MODES OF OPERATION

1. Dynamic VAR compensator (No AC drives connected)-- Generally, a fixed reference is used (often 0) and a VAR transducer is attached to the feedback input. The transducer measures the Reactive Volt Amperes at the input to the system, feeder, or sub-station. This signal applied to the feedback input of the PI regulator will generate the right amount of reactive VAR current out of the source so that the total reactive power at the transducer's measuring point is kept to a minimum (or whatever reference is set.)
2. Fixed VAR compensator (No AC drives connected)--In this mode, no sensor is required. The desired (fixed) amount of reactive current is set on a fixed set point aimed at the reference input to the PI regulator. Since no feedback is supplied, the integral and feedback gains of the PI regulator are both set to 0 and the reference gain is set to 1.0. In this mode, the source excretes a fixed amount of (leading) reactive power whenever it is operating. The reference input of this fixed VAR regulator is generally set by the internal setpoint, resulting in an AVERAGE power factor of near unity.
3. AC Drive source with dynamic VAR compensation (for auxiliary and/or DC Drive Loads)--In this mode, no sensor is required. As in the above Fixed VAR compensator, Feedback and Integral Gains of the PI regulator are set to 0 and

Reference gain is set to 1.0. If compensation is to be supplied for DC drives on the same feeder, the approximate reactive power reference can be calculated for each DC drive from the horsepower and DC voltage feedback signals from each drive. This will generally be done in a PLC or in the ACL card in the drive or source rack. The calculated reactive power values for each drive are added together and used to calculate the correct reactive current reference. This is then sent to the reference input of the reactive current regulator as a LAN variable. Auxiliary lighting and induction motor loads can be computed based on the contactor closure information and added to this signal or may be set as a fixed offset in the Reference Command Offset (*Iy reference adjust*) where it is added to the reference variable. The drive will supply the required compensating VARs within its operating limits. The connected AC drive power demand takes priority over the VAR command. The VAR output is therefore limited during times of drive peak power demand when overall current levels would exceed the rating of the unit. The level at which this limiting occurs is set by the Maximum Reactive Current Limit (*Max cur mag allowed*) and changes dynamically as the drives' power demand changes.

4. AC Drive source with dynamic system VAR regulation (for auxiliary and/or DC Drive Loads)--This mode requires a sensor and uses the full PI regulator to keep overall VARs to a minimum. The operation of this mode is similar to the Dynamic VAR Compensator (No. 1 above), except that there are AC drives attached to the source that are also demanding real kW power from the source DC bus output. The system is programmed to give priority to the drive power demands. This means that at peak power demand from the drives, the VAR compensation will necessarily be limited to something less than the level commanded by the PI regulator. The level at which this limiting occurs is set by the Maximum Reactive Current Limit (*Max cur mag allowed*), and changes dynamically as the drives' power demand changes. In this mode, the reactive current reference command is typically set to zero or some small negative value so that some minimum lagging power factor is maintained.

ADJUSTMENTS

The following notes give some brief guidelines as to how the various parameters of this function should be set up for successful operation.

1. Reactive Current Reference Command and feedback--These commands can be in the form of many units, but must be scaled by the "Reference Command and Feedback Scale factor" (see below). These commands must be positive to indicate leading reactive current and negative to indicate lagging reactive current.
2. Reference command and Feedback Scale factors --These scale factors convert the units of the input variables (e.g. volts of A/D input signal) to Amps RMS of reactive current desired out of the source. Divide the number of amps of reactive power required by value of the input reference or feedback for that no. of amps and set that as the scale factor.
3. Reference Command Offset (amps RMS)--Is in amps of offset (+ = leading, - = lagging) which is added to the input reference variable as a fixed offset.
4. Input Reference and Feedback Addresses--Must be set to point the appropriate variables to the reference and feedback inputs to this function. If these functions are not used, these may be set to "unused variable".
5. Input Reference Command Slew Rate (amps/sec.)--Can be used to limit step reference input rate of change, stabilize external control, or eliminate high frequency noise on the circuit. Normal recommended setting is 10,000 amps /sec., which essentially disables the slew limit.

6. PI regulator gains (actual gain factors)--In some modes where the reference is “passed through” to the inner loop, the Integral and feedback gains are set to 0 and the reference gain to 1.0. This essentially disables the PI regulator. In cases where the PI regulator is used, these gains must be set to obtain stable operation with the reference and feedback elements used in the system. Typical gains for a 5 radian response might be 20 for the reference and feedback proportional gains and 100 for the integral gain. For a first order response, the feedback and reference proportional gains should always be equally set. For second order responses--if the reference gain is set lower than the feedback gain, over damped response occurs and if set higher, under damped response occurs.
7. Integrator limits (amps RMS)--These are anti-wind-up limits on the integrator. There are independently adjustable positive and negative limits. Normally the positive and negative limits should be set for the same value. While the setting of these limits is not critical, it should never be set lower than the Maximum Reactive Current Limit or respective Fixed Reactive Current Limit settings.
8. Maximum Reactive Current Limit Setting (amps RMS) (NOT USED FOR COMPENSATOR MODES IF NO DRIVES ARE CONNECTED)--This limit needs to be set so that the total current capabilities of the source hardware are not exceeded. Arriving at a proper setting will generally require a system and/or duty cycle analysis of demand on the source. When active, the actual limit on the reactive current is dynamically set by the following equation:

$$\text{Internal } I_y \text{ fbk} = \sqrt{(\text{Max cur mag allowed})^2 - (I_x \text{ cmd avg})^2}$$

Where *Internal Iy fbk* is the overall reactive current limit, *Max cur mag allowed* is the maximum reactive current limit, and *Ix cmd avg* is the real current component demand of the drives connected to the source DC output bus (calculated dynamically). Typical settings for Maximum Reactive Current Limit are about 70-110% of rated current for the source.

9. Reactive Current Limit Filter (rad./sec.) (NOT USED FOR COMPENSATOR MODES IF NO DRIVES ARE CONNECTED)--May be used to stabilize the dynamic limit circuit as needed. Recommended setting is 100 rad./sec.
10. Fixed Reactive Current Limits (amps RMS)--These limits are the reactive current limits for the reactive VAR compensator (with no AC drives attached). They are fixed limits on the range of the reactive current reference command and are generally set for about the rated amps of the source (since all current is essentially reactive current in this case.) In known duty cycle applications, this limit may be set somewhat higher than rated amps.

Vector Rotate & PWM Modulator

These functions provide the interface between the control regulators and the power converter and ac line. Terminal ac voltages, ac input currents, and dc volts are transduced and converted to the regulator’s vector domain to be used as feedbacks. The PWM modulator translates x-y regulator commands into a-b-c PWM on/off commands to the power devices.

There are no adjustable parameters in these functions. All parameters are automatically set by the Source commissioning procedure.

Voltage Reference

The Voltage Reference function has no user parameters, but user diagrams allow visibility to the reference structure.

The following variables represent the final values calculated by the control for this function and also the output of the function.

Variable	Description
<i>DC voltage reference</i>	Dc link voltage reference calculated by the control as a function <i>Max lineup output</i> , the required rms motor voltage of the drives that are supplied by the source.
<i>DC voltage slew rate</i>	The control calculated slew rate of the dc link. This value is used to control the rate at which the control brings up the dc link to <i>DC voltage reference</i> once.
<i>Inner reg enable</i>	Commands the inner regulators to run. This happens at the same time that the bridge is enabled.
<i>DC bus feedback</i>	DC link voltage feedback. Used here to precondition the ramp when the source is not running.
<i>Vreg volt ref</i>	The output of the voltage reference function.

The Voltage Reference provides the desired dc link voltage command to the Voltage Regulator. In normal operation this is a fixed constant. The value of the voltage reference, *Vreg volt ref*, is determined during commissioning time by the user-entered value, *Max lineup output*. The control calculates the reference through the following rule, provided that the value entered was within the allowed range.

$$DC\ voltage\ reference = 1.10 * \sqrt{2} * Max\ lineup\ output$$

Example: for *Max lineup output* = 575V nominal input voltage, *DC voltage reference* will be 894Vdc.

The nominal AC line input voltage can be within the range of 460V to 575volt to provide a dc link from range of 715.56 to 894.49

Note that the PWM source boosts the dc voltage higher than nominal rectified line voltage. This is fundamental, if the ac voltage increases to too high a level, the PWM Source's ability to control power factor and distortion is degraded. For this reason, where possible, it is best to have a lower ac input voltage and a higher *Max lineup output* (e.g. 460 volt ac line and a *Max lineup output* of 575).

The reference is modified prior to starting pwm action, when *Inner reg enable* is False, in order to match the existing rectified ac voltage level. At pwm startup, when *Inner reg enable* becomes True, the reference is ramped to its nominal value, *DC voltage reference* at the rate determined by *DC voltage slew rate*.

Not shown on the simplified block diagram, the reference is temporarily modified during line transients.

There are no adjustable parameters in the Voltage Reference function; all parameters are automatically set by the source commissioning procedure.

Voltage Regulator

The Voltage Regulator has a proportional and integral (P-I) structure that controls the dc link voltage. The proportional path provides quick response to dc voltage changes (typically from dc load changes or ac line transients) while the integral path

forces the link voltage to match the Voltage Reference in steady state. The integrator does not windup if subsequent limits prevent regulation.

The output of the Voltage Regulator becomes the real current command into the PWM source's fast inner Current Regulator.

There are no adjustable parameters in the Voltage Regulator function, all parameters are automatically set by the source commissioning procedure.

The Voltage Regulator function has no user parameters, but user diagrams allow visibility to the structure.

The following variables are mirror images of final values calculated by the control for this function. The main output of the function is also shown.

Variable	Description
<i>DC voltage feedback</i>	Voltage regulator feedback. It is the output of a FIR filter which conditions <i>DC bus feedback</i> .
<i>Vreg volt ref</i>	The voltage regulator reference. It is slewed from the ac line rectified value at the time the start command is given to the calculated regulation level. It remains constant except for some quick slew backs during line transients. See the functional description, <i>Voltage Reference</i> .
<i>Vreg crossover gain</i>	The voltage regulator bandwidth. This is a function of the current regulator bandwidth and the execution rate of the regulator.
<i>Total capacitance</i>	Total bridge capacitance of the source bridge only. This is not the total capacitance seen by the source. The source voltage regulator is tuned so that it can meet dc link regulation specifications with as much as five times the capacitance of the source. <i>Total capacitance</i> is not modified as the capacitance seen by the source increases.
<i>Vreg crossover comp</i>	The fundamental bandwidth compensation for the voltage regulator. It is $(2/3 * Vreg\ crossover\ gain * Total\ capacitance)$.
<i>Vreg prop gain</i>	Voltage regulator proportional gain.
<i>Vreg integral gain</i>	Voltage regulator integral gain. This is a function of the voltage regulator bandwidth.
<i>Ix cmd pos limit</i>	The positive current clamp for the voltage regulator. If the current command is hitting the clamp, the integrator will freeze in the direction so it will not make the condition worse. Also, the clamped condition will begin a regulator limit timer that will result in the alarm, <i>Regulator in limit</i> . If the conditions persists, the source will trip with <i>Reg in lim time out</i> .
<i>Vreg integral</i>	The voltage regulator integrator.
<i>Ix cmd neg limit</i>	The negative current clamp for the voltage regulator. If the current command is hitting the clamp, the integrator will freeze in the direction so it will not make the condition worse. Also, the clamped condition will begin a regulator limit timer that will

result in the alarm, *Regulator in limit*. If the conditions persists, the source will trip with *Reg in lim time out*.

Real cur command The output of the voltage regulator, which is also the input to the x-channel of the current regulator.

Phase Lock Loop Function

The source phase lock loop function is the heart of the source control. The pll outputs phase and frequency information to the rest of the control that is critical to the regulators and gating. As with the other source regulation functions, there are no user parameters that directly effect the regulator, but there are some commissioning wizard parameters that are critical.

In order for the source phase lock loop to accurately lock to the ac line under all types of loading conditions, information about line stiffness, inductance and resistance must be known. The most vital information needed for the source phase lock loop conditioning and current regulator gains is ac line inductance. The control can calculate inductance from user-provided transformer information and know bridge inductance information, or the user may enter the inductance and bypass those calculations. The most fundamental user parameters are listed below.

Parameter	Description
<i>Transformer KVA base</i>	The KVA rating of the transformer feeding the source – used in the control’s inductance calculation.
<i>Xfrmr per cent res</i>	The per cent resistance of the transformer feeding the source. This value is usually not critical to performance and for that reason can be left at zero.
<i>Measured Inductance</i>	The user-measured inductance of the source’s feed. If this value (default of zero) is non-zero, then it becomes the value of inductance used by the control to calculate pll compensation and current regulator gains. If this value is zero then the control uses the inductance it calculates from <i>Transformer KVA base</i> and <i>Xfrmr per cent imped</i> .
<i>Xfrmr per cent imped</i>	The per cent impedance of the transformer feeding the source. This value can be increased from name-plate data if feeder lines are very long.
<i>AC feeder source</i>	Determines the bandwidth of the phase lock loop. If the “utility” selection is used, the bandwidth is set to obtain an amount of “sluggishness” appropriate for a utility feed. The pll will be more robust and less sensitive to un-real disturbances. The setting should be “isolated generator” only if the line is a diesel-generator or other spongy line source. The bandwidth ratio of “utility” versus “isolated generator” is 4:1.
<i>Phase rotation req</i>	The phase lock loop can lock to either “forward-ABC” or reverse phase sequence. The fault, <i>AC line rev phs seq</i> will occur if the wrong sequence is seen by the control.
<i>AC input voltage</i>	The line to line voltage input is a major determination of the phase lock loop gains.

Input frequency The phase lock loop regulator clamp settings are determined by this input.

The following table lists and describes several variables associated with the phase lock loop.

<i>Variables</i>	<i>Description</i>
<i>Y axis line voltage</i>	The feedback for the phase lock loop regulator. The reference is zero, since the phase lock loop is attempting to regulate the y-component of the line voltage to zero.
<i>X axis line voltage</i>	The demodulated x-axis component of the ac line voltage. It is not used in the actual phase lock loop regulator, but is used with VyLine to calculate the AC line magnitude, <i>AC line voltage</i> .
<i>PLL error</i>	The phase lock loop regulator error.
<i>Line monitor frq</i>	A low-pass filtered version of the phase lock loop frequency. It is used for frequency fault checking.
<i>PLL frequency</i>	The main un-filtered ac line frequency, as determined by the phase lock loop regulator. This value is used throughout the control's regulators.
<i>AC line angle cmd</i>	This is the angle of the ac line as determined by the phase lock loop regulator, and is used to determine the phase of the up/down commands to the bridge gating interface.
<i>AC line angle fbk</i>	This is the angle of the ac line as determined by the phase lock loop regulator, and is used to demodulate the voltage and current feedbacks at the beginning of each fast execution task.
<i>PLL prop gain</i>	The phase lock loop proportional gain. This gain is dynamic. It very hot before the pll is locked, and then changes to a more sluggish gain.
<i>PLL integral gain</i>	The phase lock loop integral gain. This gain is dynamic. It is very hot before the pll is locked, and then changes to a more sluggish gain.
<i>PLL max frequency</i>	Maximum frequency allowed by phase lock loop regulator. This is function of the nominal input frequency.
<i>PLL min frequency</i>	Minimum frequency allowed by phase lock loop regulator. This is function of the nominal input frequency. It is also dynamic. When the pll is not locked, this variable is set to the negative of <i>PLL max frequency</i> .
<i>PLL proven</i>	This Boolean indicates whether the pll is locked. It is used throughout the control as a permissives to run or check various protections.

Regulator Limits

Each regulator has limits that are used to protect against wind-up and excessive demands for the output of the regulator. See *Regulator in limit* or *Reg in lim time out* for details.

Control Diagnostic Variables

Several filtered control diagnostic variables are available to the user. They are listed in the table below.

<i>Variable</i>	<i>Description</i>
<i>AC line current</i>	Filtered current magnitude. A true magnitude calculation of demodulated Ia and Ib which is then filtered.
<i>AC line voltage</i>	Filtered ac line magnitude. A true magnitude calculation of Vab and Vbc which is then filtered.
<i>AC line frequency</i>	The filtered ac line frequency produced by the phase lock loop.
<i>DC bus power</i>	The dc bus power is calculated from the demodulated ac line voltages and currents, and is compensated for bridge losses.
<i>DC bus current</i>	The filtered, estimated dc link current. This is calculated from <i>DC bus power</i> divided by the dc link voltage.
<i>AC line input power</i>	Filtered ac line power. This is the power at the terminals of the source. It is calculated from the demodulated currents and voltages sensed at the terminals of the source.
<i>Volt amps reactive</i>	This is the filtered volt-amps reactive seen by the source control through the demodulated voltages and currents measured at the terminals of the source.
<i>Charge res temp</i>	The filtered, estimated temperature of the charge resistor. All three charge resistor temperatures are modeled. This temperature is the maximum of the three.
<i>Ground current</i>	The filtered zero sequence current. This filtered value is an indication of the ground current seen by the source control.

Notes

Chapter 3 Wizards

Introduction

This chapter contains descriptions and help items associated with configuring and diagnosing the Innovation Series low voltage-ACCBR-A series drives. They are organized in the following manner:

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Simulator Setup

Simulator Setup: Introduction

The *Simulator Setup* configures the drive to run in simulator mode.

Simulator Setup: Simulator Mode

If you would like to run the drive in simulator mode, select Yes.

If you do not want to run the drive in simulator mode, select No.

Related functions

- *Simulator*

Simulator Setup: Hardware Fault String Override

If you would like to disable the *Local flt* and *System flt* trip faults in simulator mode, select Yes.

If you would like to continue to check for the *Local flt* and *System flt* trip faults in simulator mode, select No.

Related functions

- *Hardware Fault Strings*

Simulator Setup: Conclusion

The *Simulator Setup* has reconfigured the drive with your selections.

Analog Filter Setup

The *Analog Filter Setup* wizard directs configuration of the analog input filters. For more information on the analog input filters, see the *Analog Inputs/Outputs and Mapping* function help.

Capture Buffer Setup

The *Capture Buffer Setup* wizard directs configuration of the capture buffer. For more information on the capture buffer, see the *Capture Buffer* function help.

DAC Setup

The *DAC Setup* wizard directs configuration of the analog outputs (DACs). For more information on the DACs, see the *Analog Inputs/Outputs and Mapping* function help.

Diagnostic Filter Setup

The *Diagnostic Filter Setup* wizard directs configuration of the general purpose diagnostic filters. For more information on the diagnostic filters, see the *General Purpose Filters* function help.

Ground Fault Setup

The *Ground Fault Setup* directs configuration of the ground fault protection. Allowing the control to calculate the default ground fault parameter settings is recommended. For more information on the ground fault parameters, see the *Ground Fault Protection (Slow)* and *Ground Fault Protection (Fast)* function helps.

Panel Meter Setup

The *Panel Meter Setup* wizard directs configuration of the panel meters. For more information on the panel meters, see the *Analog Inputs/Outputs and Mapping* function help.

Per Unit Setup

The *Per Unit Setup* wizard directs configuration of the per unit parameters that determine scaling for the DDI. Allowing the control to calculate the default per unit settings is recommended.

Relay Output Setup

The *Relay Output Setup* wizard directs configuration of the relay outputs. For more information on the relay outputs, see the *Digital Inputs/Outputs and Mapping* function help.

Remaining Parameter Setup

The *Remaining Parameter Setup* wizard directs configuration of parameters that cannot be assigned default values during the commissioning process. Allowing the control to calculate the default parameter settings is recommended.

Default Parameter

You may choose between selecting the default parameter calculations (to be made by the control) or individually picking each of the parameters associated with this function. Generally, the best choice is to allow the control to calculate the parameter values. Setting each individual parameter by hand requires the user to be much more familiar with the function. Proceed with caution when choosing this path.

Source Commissioning

Source Commissioning: Overview

The *Source Commissioning* wizard guides the user through the process of configuring the regenerative source for a particular application. It asks a series of questions that allow the user to specify important control parameters. It also directs the control to perform calculations to determine the values of other parameters. As the wizard is completed, the source should have all of the information to run successfully.

The *Source Commissioning* wizard may be run more than once, with the following note of caution.

Some of the parameters that are changed by rule calculations may be modified after the wizard finishes. If any parameter modifications have been made, they may be lost when the *Source Commissioning* wizard runs. Parameter changes should be reviewed each time the wizard runs. In addition, making a parameter backup prior to running the wizard is highly recommended.

Source Commissioning: Unit Systems

Three different unit systems are available for displaying parameters and variables:

- *Imperial (English)*
- *Metric (SI)*
- *Native (Platform)*

The *Native (Platform)* unit system displays parameters and variables in the same units that the internal control uses.

Select one of the three unit systems.

Related functions

- *Language and Units Presentation*

Source Commissioning: Known Inductance

In certain cases, you may already know the inductance of the feeder, and may trust this value more than this transformer data. This value may have come from a previous manual tune test. Whenever *Measured Inductance* is set to a non-zero value, the inductance calculated by transformer data will not be used. Setting *Measured Inductance* back to zero will allow use of the inductance calculated by transformer data.

Source Commissioning: Transformer Data

The source uses R/L compensation to lock to the true ac line. In order to correctly lock to the line, proper inductance information is especially needed. Current regulator gains are also heavily dependent upon inductance. The wizard's questions allow the control to calculate inductance provided by the transformer, and add this values to its own bridge values.

This inductance is typically small compared to that provided by the source bridge itself; therefore, it is better to leave this value at zero than enter a value that is not correct. A zero entry here will usually work well, especially when the transformer feeding the source is comparatively larger.

Be sure to enter the values in the units specified in the wizard.

Since the transformer represents the bulk of the impedance to the ac line, user-provided information concerning it can allow the source phase lock loop to attach to the ac line more accurately.

The following values are requested:

- *Transformer KVA base*: The KVA of the transformer.
- *Xfrmr per cent imped*: Transformer per cent impedance. Refer to transformer nameplate. 5.0% is typical.

Source Commissioning: AC Line Characteristics

This help covers three items concerning the source commissioning wizard ac line.

Utility/Isolated Generator

AC feeder source determines the gain used by the phase lock loop. For almost all applications, this should be set for UTILITY. If the ac line is provided by an isolated generator, then select that option. This will provide for a more robust regulation system in case the ac line is sluggish. Selecting the isolated generator forces hotter gains on the phase lock loop so it can track the faster moving, less stable ac line.

Forward/Reverse Phase Sequence

Phase rotation req allows the user to specify the rotation direction of the ac line. A fault will occur if the requested direction of rotation is not seen by the control when the phase lock loop locks. The forward direction here is defined as A-B-C. See *ac line rev phs seq*.

Input Frequency

Input frequency is the nominal frequency of the ac line.

Source Commissioning: Output Voltage

RMS AC Line Input

AC input voltage is the ac line input voltage. This is the nominal voltage. The ac line can be “high” or “low” relative to nominal. This helps determine phase lock loop gains, as well as the protection thresholds for ac line magnitude.

RMS Inverter Motor Voltage

Max lineup output specifies the maximum ac voltage that exists in the system containing the DC source, drive, and motors. This voltage must be set correctly. It will determine the regulated dc link voltage. Internal protection prevents the dc link regulation setpoint from being set higher than is safe for the bridge. A zero entry can be used here to result in a dc link voltage; the maximum for the bridge. This can be used when the source is used in “line compensation” mode, and no drives are attached to the source. The source will always provide more operating margin when the dc link is high compared to the ac line. A 460 volt input and a 575 volt output is a favorable setup. The dc link regulation setpoint is calculated as $1.1 * \sqrt{2} * \text{Max lineup output}$, as long as the result does not exceed the maximum allowed dc link voltage setpoint for the bridge.

Source Commissioning: Source Run Pointer

Source Run Pointer

Hardware run ptr is a pointer that can be directed to a digital input (LAN input, ect.) The designated input can then control start and stop of the source. If the input is high at power-up/reset, the source will begin the running process immediately after power-up, provided that all other permissives are met. Once the source is powered up, the source will run/stop based on an edge detection of the input. Rising edges cause the source to start, and falling edges will cause the source to stop.

Digital input 1 is the default setting for this pointer. If the default value is used, and nothing is tied to digital input 1, the source will not run or stop using this input.

Source Commissioning: Auto Rule Calculation

Primary Rule Calculation

This step is mandatory. It drives all of the user-answered questions into the control and forces calculation of all of the rules.

Source Commissioning: LPPA Option

Line Protection Module

The line protection module is optional. See *Line Protection Module*.

Source Commissioning: Control Auto Calculate

Let the control do it for you

Answering yes is highly recommended. The alternative will be much more difficult because it will require the user to run several different wizards, and answer questions within each of those wizards. Answering yes will allow the control to populate these several user level parameters with values based on the answers given to the proceeding questions in the wizard. The internal parameter, *Use default settings*, is used to activate this path, but actual access to this parameter is not needed.

Simulator Wizard: Simulator Introduction

You may use this wizard to reset all of the simulator user-level parameters to the factory recommended settings, or use it to examine each simulator parameter, one by one.

Simulator Wizard: Simulator Default Decision

Answering yes is usually recommended. However, if you would like to use this wizard to set a simulator parameter to a non-standard value (perhaps in order to explore the result of mis-matches between the control and the plant) answering no will provide that opportunity. *Default simulator* is used to activate this path, but actual access to this parameter is not needed.

Simulator Wizard: Simulator Enable Decision

A simulator mode is available in the drive. The simulator mode allows the drive to be “run”, while not necessarily attached to an ac line or to a drive. A simulated ac line is produced, which gives user capability to cause transients. The user can also request that a dc current be applied to the dc link. See *Simulator*.

Simulator Wizard: Simulator Local/System Fault Options

Two protective hardware circuits must be satisfied to allow cell firing, which allows the drive to run. They are *Local fault string* and *System fault string*. These protective strings can be ignored for the purpose of running the drive in simulator mode. If they are not ignored, they must be satisfied to make the source run as a simulator.

Simulator Wizard: Simulator Basic Bridge Parameters

These simulator parameters represent the most basic “plant” values. They can be set to a value that is different from the control’s compensation to explore the effects of a mis-match between the control and the plant.

- *Sim line resistance* - Represents the plant resistance in inductors, cables, and transformers.
- *Sim line inductance* - Represents the plant inductance in inductors, cables, and transformers.
- *Sim capacitance* - Represents the capacitance of the source bridge in addition to the capacitance of all of the simulated attached drive bridges.

Simulator Wizard: Simulator Voltage and Frequency

These simulator parameters represent the control’s perspective of the ac line attributes.

- *Sim line frequency* - Determines the frequency of the simulated ac line. This parameter again allows mis-match between the frequency, which the source expects to see, and the actual simulated frequency.
- *Sim line voltage* - Determines the magnitude of the ac line simulated voltage. This parameter allows simulation of high and low line conditions.

Source Commissioning: Wrap-up

Usually, there will be faults remaining after the commissioning wizard has reached this point. These faults are a result of the control continuing to run its protective functions during the commissioning exercise. The simplest way to clear these faults is to give a hard reset to the control.

Source Commissioning: Capture Buffer Re-arm

Pushing this button will re-arm the capture buffer if the trigger condition is not presently met. If the defaults were used, the capture buffer will be set to trigger on a trip fault. Therefore, if a trip fault still occurs, pushing the button will not actually re-arm the buffer. **It should be re-armed after there are no faults. This may be after the hard reset.** If the capture buffer is set to trigger on a trip fault, it will be armed the first time it powers up after a hard reset without a fault.

Source Commissioning: Completion

You are finished. The source should be ready to run. Be sure to issue a hard reset after loading up all of the changes.

Reactive Current Setup: Drive Supplier?

Most regenerative sources are used for supplying power to one or more drives. For this case, the control must limit use of user-requested reactive current to a point that

will not interfere with drive operation. Answering yes to this question will allow the control to enforce this limitation.

Reactive Current Setup: Introduction

This wizard will look identical to that part of the drive commissioning wizard pertaining to Reactive Current Setup. It is added here for convenience. You may run this wizard without forcing the control to re-calculate all other rules. Either path will work.

Reactive Current Setup: Unity Power Factor?

Choosing “Src Unity PF” here will result in a zero reactive current reference. The source will then regulate unity power factor.

Related functions

Reactive Current Reference

Reactive Current Setup: Voltage/Current Regulator

You have chosen to operate in a mode other than unity power factor. This means that you will be using the reactive current regulator in a mode other than simply regulating zero reactive current. You now have two choices: regulate reactive current to control power factor (or simply command a fixed amount of reactive current to load the source) or use the source as an ac line voltage regulator. The voltage regulator mode requires a special internal inductor.

Related functions

Reactive Current Reference

Reactive Current Setup: Invalid Voltage Reference Entry

You have chosen to operate the source as an ac line voltage regulator. Choosing *Iy ref volt setpt* will allow the control to accept a user-entered, fixed reference for ac line voltage.

Do not choose *Iy ref cur setpt* or *LAN Iy ref*. These are not valid entries for voltage control. Go back and choose a proper reference.

Analog input 1 should be used when the voltage reference is coming from an external input provided by a voltage reference. This reference can be read by the vco input and then scaled internally by this regulator.

Related functions

Reactive Current Reference

Reactive Current Setup: Voltage Regulation Setup

You have chosen to regulate ac line voltage with a fixed voltage reference. This parameter is that fixed reference. Be sure to select a reasonable value.

Related functions

Reactive Current Reference

Reactive Current Setup: Voltage Command Scale Factor

Since the internal part of this regulator is designed to be scaled as current, a scale factor is needed here to convert the voltage reference to a current.

Related functions

Reactive Current Reference

Reactive Current Setup: AC Line Voltage

You have chosen to use the source as an ac voltage regulator, and to use an analog input to receive that reference. Now, in order for the control to scale that voltage correctly, enter the line to neutral peak voltage represented by 1.0 volt at the input to the control.

Related functions

Reactive Current Reference

Reactive Current Setup: AC Voltage Reduction

If you allow voltage reduction, the output of the reactive current regulator will be allowed to go all the way to the negative of rated current for the source. If you do not allow it, then the output will not be allowed to go below zero.

Related functions

Reactive Current Reference

Reactive Current Setup: Reactive Current Setpoint

In the reactive current mode, there are various ways to select the setpoint.

- *Iy ref volt setpt* is **not one of these**. If you have chosen it, go back and enter a valid entry.
- *Iy ref cur setpt* should be chosen when it is desirable to command the source to run with a fixed amount of reactive current. This is useful in testing the source or for any reason where it is desirable to load the source with a fixed amount of current or in the case where a drive is not connected to the terminals of the source. Note that care must be taken as to not exceed the rating of the transformer that is feeding the source.
- *LAN Iy ref* is to be used when the lan is providing the reactive current reference. See [\[\[LAN Signal Map\]\]](#)
- *Analog input 1* is to be used when the current setpoint is being provided by an external voltage reference. Note that it must later be scaled to convert to a current reference.

Related functions

- *Reactive Current Reference*

Reactive Current Setup: Fixed Current Reference

This is the fixed current reference. This value of current will be regulated within the capability of the source. Note that the source has much more ability to provide this current when the reference is negative..

Related functions

- *Reactive Current Reference*

Reactive Current Setup: Analog Input Current Reference

Provide here a to-scale factor to be used in converting the analog input voltage to current. Enter the value of **peak** amps for 1.0 volt of input at the control. This scaling is necessary in order to keep the internal part of the regulator in units of amps.

Related functions

Reactive Current Reference

Reactive Current Setup: Current Feedback Address

In the reactive current mode, there are various ways to select the reactive current feedback:

- *Avg line voltage mag* **is not one of these**. If you have chosen it, go back and enter a valid entry.
- *Internal Iy fbk* should be chosen whenever it is desirable to use the control's reactive current feedback. In this case, the control attempts to follow the reactive current reference without any external feedback, such as Lan or analog inputs.
- *LAN Iy fbk* is to be used when the lan is providing the reactive current feedback.. See *[[LAN Signal Map]]*. Note that this is most likely when the lan reference is also used.
- *Analog input 2* is to be used when the current feedback is being provided by an external voltage reference. Note that it must later be scaled to convert to a current reference. Note that this is probably used when the *Analog input 1* is used for the reactive current reference.

Related functions

- *Reactive Current Reference*

Reactive Current Setup: Fixed Current Analog Input Scaling

You have chosen an analog input as the feedback to the reactive current regulator. You must now enter the scale that input so as to convert it to a current signal. Enter the peak amps equivalent to 1.0 volt on the analog input.

Related functions

Reactive Current Reference

Reactive Current Setup: Maximum Allowed Current

This value is the maximum reactive current that you want to allow out of the reactive current reference regulator. The reactive current clamp (of the inner regulator) is coordinated with this setting.

Related functions

- *Reactive Current Reference*

Reactive Current Setup: Auto Rule Calculation

This must be done to force the run of the reactive current regulator rules. These rules will take the provided inputs to this wizard and produce the needed internal calculations.

Source Sequencer Wizard: Default Sequencer Setup

Answering yes is usually recommended. However, you can use this wizard to set up sequencer parameters to non-standard values. This switch may also be used to re-set the sequencer parameters to the factory recommended values.

Source Sequencer Wizard: Fault Reset and Hardware Run Addresses

These two pointers determine where the control looks to receive fault reset and hardware run commands. A fault reset can also be done from the keypad.

- *Fault reset select* - Aiming this parameter towards an input will allow the input to reset trip faults to the source.
- *Hardware run ptr* - Aiming this parameter towards an input will allow the input to control the start and stop of the source. If this input is high when the source boots up from a hard reset, the source will begin the start sequence. Afterwards, this input will then start/stop the source on rising/falling edges of that signal.

Source Sequencer Wizard: Wizard Completion

You have completed the source sequencer wizard. The source is ready to run again with the new inputs (be certain there are no faults).

AC Line Protectives Wizard

Line Protection: Introduction

The Line Protection Setup Wizard allows selection or restoration of the control calculated parameters that affect line protection functions concerning over and under frequency, as well as over and under voltage. Selecting the value of each parameter is also an option.

Line Protection: Default Settings

Choosing the Line Protection Setup Wizard defaults are highly recommended. Making the default selection will result in voltage and frequency protection settings. These are in line with the specifications of the source and are proven settings.

Line Protection: Overvoltage

These parameters set the level of protection for ac line over-voltage. Using the control default values, as calculated in the previous steps, is highly recommended (you can go backward).

- *Line OV fault lvl* - ac line voltage - the source will trip above this.
- *Line OV alm on lvl* - ac line voltage - the source begins to alarm the over-voltage condition above this.
- *Line OV alm off lvl* - ac line voltage - the source quits alarming the over-voltage condition below this.

For additional information, see *Protective Functions*.

Line Protection: Undervoltage

These parameters set the level of protection of the ac line under-voltage protection. It is highly recommended to use the control default values as calculated in the previous steps (you can go back to review these steps).

- *Line UV fault lvl* - ac line voltage - the source will trip below this.
- *Line UV alm on lvl* - ac line voltage - the source begins to alarm the under-voltage condition below this.
- *Line UV alm off lvl* is the ac line voltage above which the source stops alarming the under-voltage condition.

For additional information, see *Protective Functions*.

Line Protection: Overfrequency

These parameters set the level of protection for ac line over-frequency. Using the control default values as calculated in the previous steps is highly recommended (you can go back to review these steps).

- *Over frq flt lvl* - ac line frequency - the source will trip above this.
- *Over frq alm on lvl* - ac line frequency - the source begins to alarm the over-frequency condition above this.

- *Over frq alm off lvl* - ac line frequency below which the source stops alarming the over-frequency condition.

For additional information, see *Protective Functions*.

Line Protection: Underfrequency

These parameters set the level of protection for ac line under-frequency. Using the control default values as calculated in the previous steps is highly recommended (you can go back to review these steps).

- *Low frq flt lvl* - ac line frequency - the source will trip below this.
- *Low frq alm on lvl* - ac line frequency - the source begins to alarm the under-frequency condition below this.
- *Low frq alm off lvl* - ac line frequency - the source quits alarming the under-frequency condition above this.

For additional information, see *Protective Functions*.

Line Protection: Conclusion

You have completed the wizard. The control is now ready to run with the new values after the parameter upload.

For additional information, see *Protective Functions*.

Line Protection Module Wizard

Line Protection Module: Introduction

The Line Protection Module Wizard allows selection or restoration of the control-calculated parameters that affect line protection module functions. These functions concern the levels of current, at which ground faults and alarms will be reported. Choosing to select the value of each parameter is also an option.

Line Protection Module: Addresses

The following four parameters configure the “front end” of the Line Protection Module code. They turn the function on/off, and determine the input addresses and voltage to current scalings of the ground current indication.

- *LPPA mode* enables/disables the function. If the module is not present, this should be disabled.
- *LPPA gnd flt scl* has potential to scale the input voltage into a current. Default, control calculated settings set this value to 1.0, leaving all internal signals in volts.
- *LPP fuse blown sel* is the control’s address of the MOV fuse indicator input.
- *LPP gnd signal sel* is the control’s address of the ground current sensing signal.

For additional information, see *Line Protection Module*.

Line Protection Module: Default Selection

In general, use the default settings. Only change the settings from defaults if you are certain that you understand the procedure.

For additional information, see *Protective Functions*.

Line Protection Module: Thresholds

The following four parameters configure the ground current signal's low pass filter, as well as the its alarm and trip threshold.

- *LPPA gnd flt fil* - response in rad/sec of the low pass filter applied to the input ground current indication signal.
- *LPPA gnd flt alm* - ground current indication signal level above which the alarm, *Ground flt alm, LP*, is given.
- *LPPA gnd flt clr* - ground current indication signal level below which the alarm, *Ground flt alm, LP*, ceases.
- *LPPA gnd flt lvl* - ground current indication signal level above which the trip fault, *Ground flt, LP*, is given.

For additional information, see *Line Protection Module*.

Line Protection Module: Conclusion

- You have completed the Line Protection Module Wizard. After an upload, the control is ready to run with those new values.

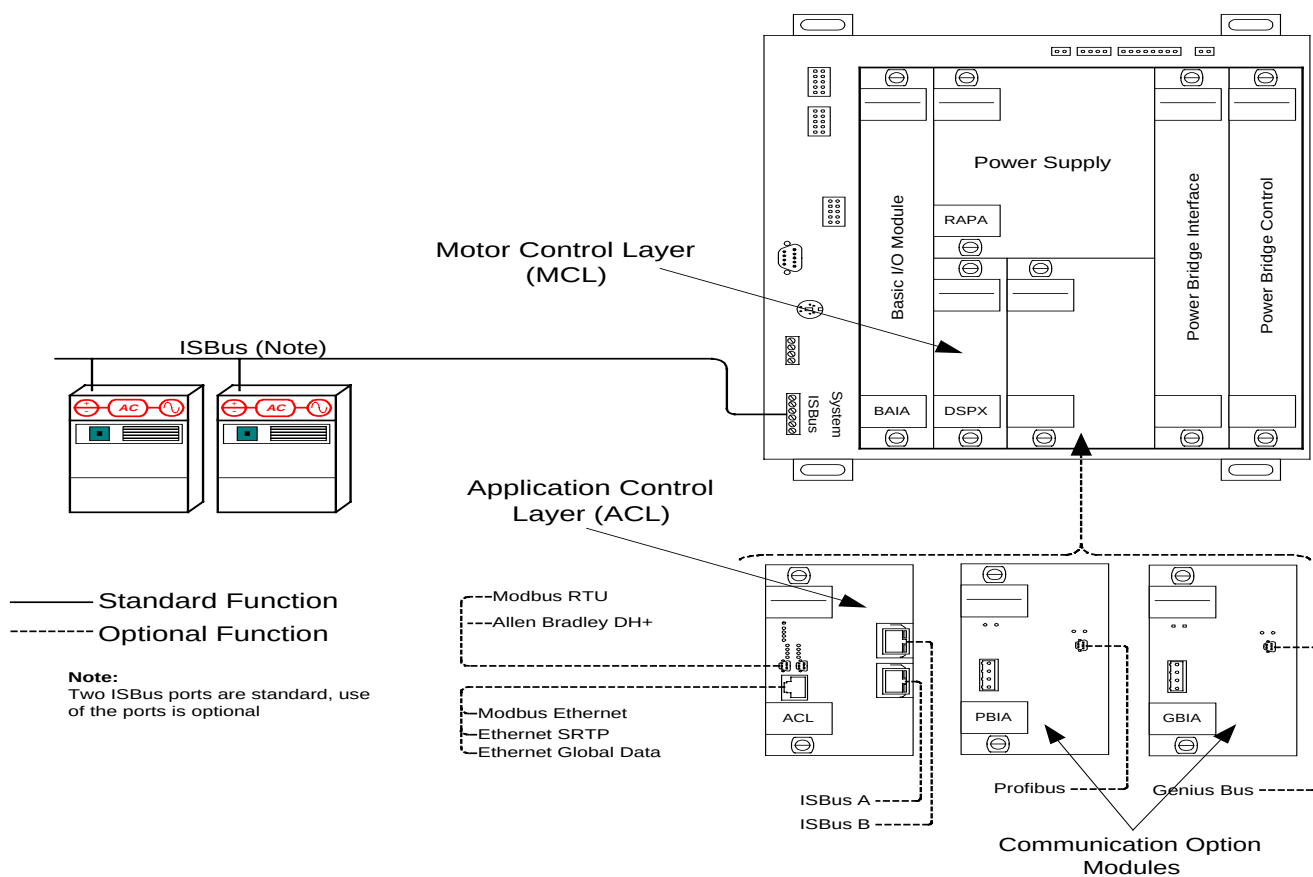
For additional information, see *Line Protection Module*.

Chapter 4 Signal Mapping

Introduction

Interfacing with the motor control layer (MCL) of the drive is done through I/O or a standard LAN (local area network) signal map. This chapter describes the standard LAN signal map which is used for several LAN interfaces (refer to the following figure and table).

<i>Section</i>	<i>Page</i>
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Variable Mapping	3
Variable Maps (Source Patterns, ACCBN-A & ACCBR-A).....	6



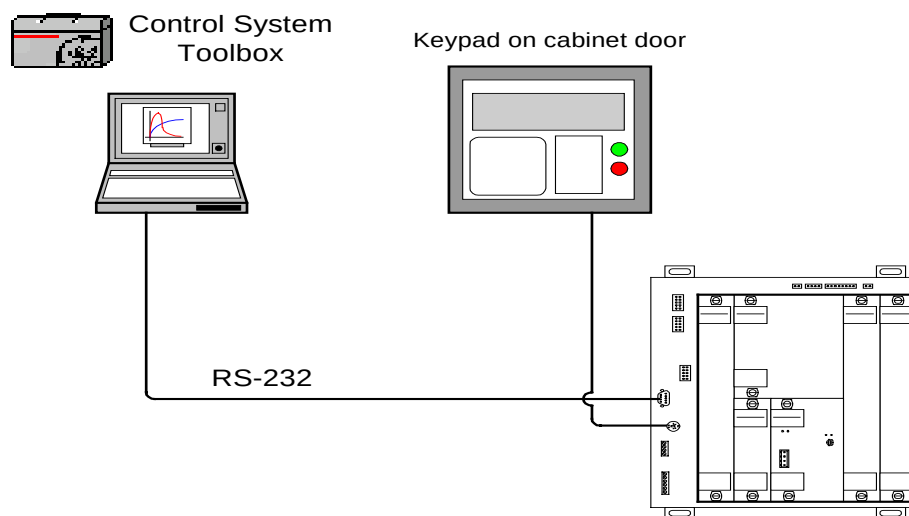
Interface	Associated Module	Notes
Profibus-DP Slave	IS215PBIA	Freeze and sync mode supported Support of 9.6Kb to 12Mb
Genius	IS215GBIA	LAN heartbeat supported
ISBus Slave	IS215DSPX	Supported from motor control layer, no additional modules required
Application Control Layer (ACL)	IS215ACLI	From the ACL, other LANs are supported: - Modbus RTU - Allen Bradley DH+ - Modbus Ethernet - Ethernet SRTP - Ethernet Global Data Configuration is required in the ACL

Parameter Configuration for Signal Mapping

The 64 byte bi-directional signal map is configured with either the keypad or toolbox.

Refer to the data sheets associated with these interface modules for a detailed description of the configuration.

Signals are LAN or I/O based variables that either control the drive or provide feedback data on the status of the drive. For example, an analog input signal provides the speed reference for the drive



Parameters are used in the drive for configuration of functions. For example, six parameters are used to configure the ramp rate function generator in the general industries pattern.

LAN Interface	Description of Configuration
Genius Bus	Auxiliary Genius Bus Interface Module IS215GBIAH_A__ GEI-100269
Profibus-DP	Auxiliary Profibus-DP Interface Module IS215PBIAH_A__ GEI-100419
ISBus	GEH-6417
ACL based LAN Interfaces	GEI-100434

Variable Mapping

Variables are dynamic references for control of the drive or contain feedback on the status of the drive. For example, speed feedback and speed reference are two variables associated with the speed regulator function in the drive

The variable map is defined in terms of paired reference and feedback pages.

Page Type	Direction of Data
Reference Page	Sent from the controller to the drive (speed reference for example)
Feedback Page	Sent from the drive to the controller (speed feedback for example)

Each element in the map is assigned a data type. Standard assignments utilize the two data types, a 32-bit real and 1-bit Boolean.

Data Type	Format
Real	IEEE 754 single format (23-bit mantissa, 8-bit exponent, 1-bit sign)
Boolean	1-bit per signal

The following table specifies variables which indicate the LAN health and status for the LAN Configuration and Health function.

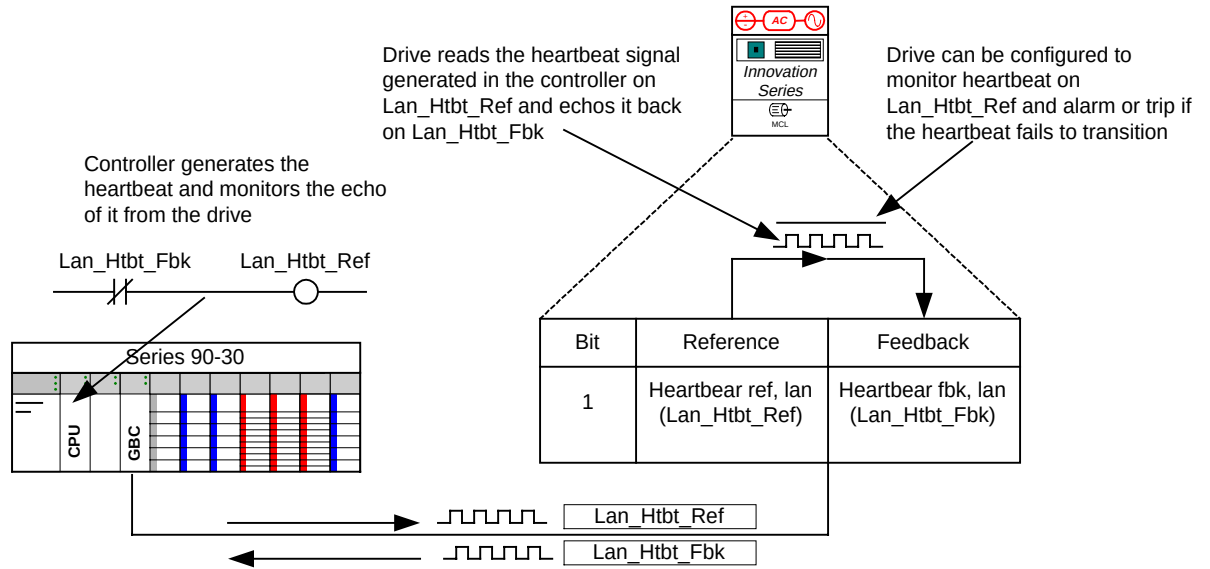
Variable	Description
LAN connection OK	Indicates that the health of the LAN connection is good, such that the LAN watchdog function is satisfied.
LAN commands OK	Indicates that the health of the LAN references are good, based upon the detection of two successive LAN connection ok indications.
Heartbeat ref, LAN	LAN heartbeat signal that is generated by the controller. The drive can be configured to alarm or trip upon the failure of this heartbeat. The drive also echos this signal back out the Heartbeat Fbk LAN variable.
Heartbeat Fbk, LAN	Drive echos the Heartbeat ref variable out on Heartbeat Fbk.
Sys ISBus error Cnt	Not applicable
Sys ISBus error Reg	Not applicable
Frame PLL OK status	Not applicable
FPLL Freq Output	Not applicable

Applying the LAN Heartbeat Echo Feature

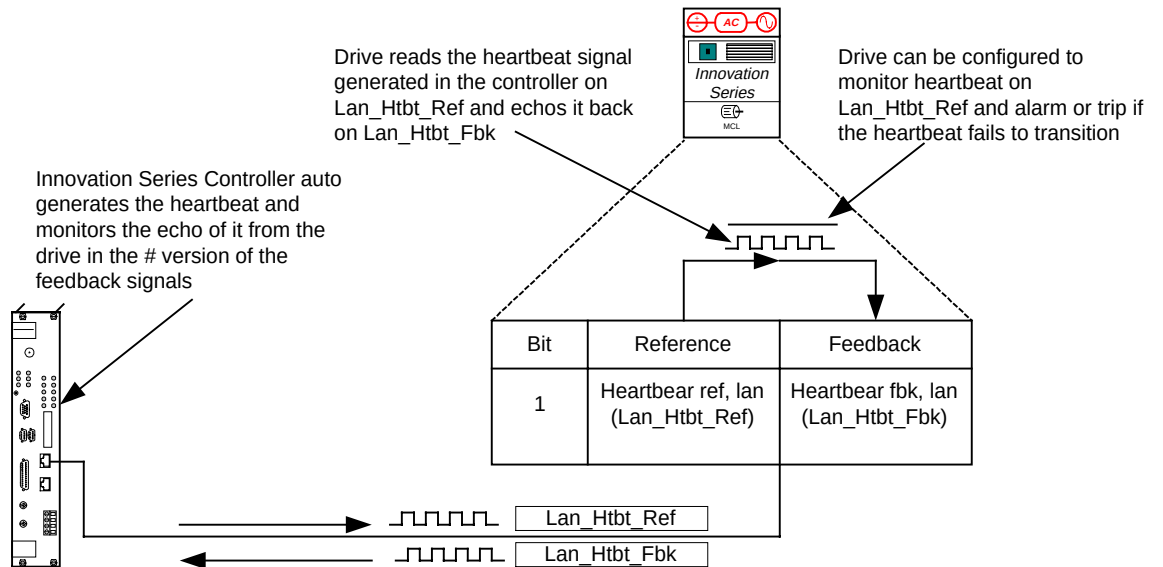
When controlling a drive over a LAN, both the controller and drive need to monitor and react to changes in the status of LAN health. The heartbeat echo feature in the drive provides a mechanism for this function.

The following illustrations of the heartbeat echo function indicate how the drive and controller obtain status on the integrity of the LAN and possible configuration options.

Heartbeat Echo Function With a PLC



Heartbeat Echo Function with an Innovation Series Controller



Application of Feedback Signals

In most control systems the LAN (Genius, Profibus-DP, etc) operates asynchronous with the execution of control logic. Two situations can occur:

- **Under Sampling** - If the control logic sweep rate is slower than the LAN sweep rate, certain samples of feedback signals from the drive are not seen by the control logic.

- **Over Sampling** - If the control logic sweep rate is faster than the LAN sweep rate, certain feedback signal samples from the drive are seen multiple times by the control logic.

To address the under sampling problem, signal conditioning is provided for dedicated *analog* feedback channels in the form of sequential averaging. Feedback signals are comprised of a series of short-term averages of the source signal. The parameter *LAN fbk avg time* configures the averaging period; updates to the feedback signal map are performed coherently.

Note that when an integer relationship exists between *LAN frame time* and *LAN fbk avg time*, then the frame and feedback averaging periods are synchronized to the extent possible. This synchronization is optimal for synchronous LAN interfaces, such as those provided by the ISBus.

Variable Maps (Source Patterns, ACCBN-A & ACCBR-A)

The following tables define the signal map for the ACCBN-A (Non-Regenerative) and ACCBR-A (Regenerative) pattern. The signal map tables provide the following as appropriate:

- 20-character user names and 12-character symbolic names
- Units or scale groups

Real Variable Map

Reference			Feedback	
Byte	Variable	Functionality	Variable	Functionality
1-4	Request bits 1, lan (Lan_Req1_Wrd)	multiple bits, see table below	Feedback bits 1, lan (Lan_Fbk1_Wrd)	multiple bits, see table below
5-8	ly reference, lan* (Lan_ly_Ref) ly_Scl *Regen Sources only	ly reference select (lyrf_Cmd_Adr) Behavior 2	Fault number (Lan_Flt_Code) <integer>	number of the active fault with (1) highest severity (trip/alarm) (2) earliest time- stamp
9-12	ly feedback, lan* (Lan_ly_Fbk) ly_Scl *Regen Sources only	ly feedback select (lyrf_Fbk_Adr) Behavior 2	AC line current, lan (Lan_I_Mag) "A rms"	=Avg[I_Mag_Fil] sequential averages
13-16	Not Used		AC line voltage, lan (Lan_Line_Mag) "V rms"	=Avg[Line_Mag_T2] sequential averages
17-20	Not Used		DC bus voltage, lan (Lan_Vdc_Fbk) Vdc_Scl	=Avg[Vdc_Fbk_T2] sequential averages

Reference			Feedback	
21-24	Not Used		DC bus power, lan (Lan_Bus_Pwr) Power_Scl	=Avg[Bus_Pwr] sequential averages
25-28	GP lan ref 01 (Lan_R01_Ref)	general purpose real var	GP lan fbk reg 01 (Lan_R01_Fbk)	GP lan fb reg 01 sel (Lan_R01_Adr)
29-32	GP lan ref 02 (Lan_R02_Ref)	general purpose real var	GP lan fbk reg 02 (Lan_R02_Fbk)	GP lan fb reg 02 sel (Lan_R02_Adr)
33-36	Not Used		AC line freq, lan (Lan_Line_Frq) Frequency_Scl	=Avg[PII_W_T2] sequential averages
37-40	Not Used		AC line vars, lan (Lan_Var_Calc) VAR_Scl	=Avg[Var_Calc] sequential averages
41-56	Not Used		Not Used	
57-60	GP lan ref 03 (Lan_R03_Ref)	general purpose real var	GP lan fbk reg 03 (Lan_R03_Fbk)	GP lan fb reg 03 sel (Lan_R03_Adr)
61-64	GP lan ref 04 (Lan_R04_Ref)	general purpose real var	GP lan fbk reg 04 (Lan_R04_Fbk)	GP lan fb reg 04 sel (Lan_R04_Adr)

Boolean Variable Map

Request			Feedback	
Bit	Variable	Functionality	Variable	Functionality
1	Heartbeat ref, lan (Lan_Htbt_Ref)	Heartbeat function: transitions expected	Heartbeat fbk, lan (Lan_Htbt_Fbk)	Heartbeat function: loopback Heartbeat ref, lan
2	Fault reset req, lan (Lan_Flt_Rst)	Fault reset select (Flt_Rst_Adr) Behavior 1, edge	No faults or alarms (No_Flt)	no active (uncleared) faults, "not (trip OR alarm)"
3	Trip request, lan (Lan_Trp_Req)	Fault.Lan trip request (Lan_Trp) Behavior 0	Trip fault active (Trip_Flt)	active trip fault, "trip"

Request			Feedback	
4	Alarm request, lan (Lan_Alm_Req)	Fault.Lan alarm request (Lan_Alm) Behavior 0	Local fault string (Loc_Flt)	local hardware permissive; bridge inhibited
5	Not Used		System fault string (Sys_Flt)	system hardware permissive; bridge inhibited
6	Not Used		Ready to Run (Run_Rdy)	device is ready & will respond to run request
7	Not Used		Bridge is on (Brg_Pwr_Enb)	bridge power is enabled;
8	Not Used		Running (Running)	sequencer task status
9-10	Not Used		<spare>	
11	X stop request, lan (Lan_Xstp_Req)	Behavior 0, level	X stop active (X_Stp_Cmd)	result of Xstop requests
12-24	Not Used		Not Used	
25	GP lan req bit 01 (Lan_B01_Req)	general purpose bool var	GP lan fbk bit 01 (Lan_B01_Fbk)	GP lan fb bit 01 sel (Lan_B01_Adr)
32	GP lan req bit 08 (Lan_B08_Req)	general purpose bool var	GP lan fbk bit 08 (Lan_B08_Fbk)	GP lan fb bit 08 sel (Lan_B08_Adr)

Appendix A

Introduction

Application firmware consists of coordinated blocks of code called **functions**. Each function performs a specific task in controlling the drive.

Parameters are adjustable values within a function that allow you to configure and adjust the drive behavior. For example, some basic parameters and their associated units include *Motor rated current* (Amps), *Motor rated freq* (Hz), *Motor rated voltage* (Volts), and *Regulator type*. Parameters can be set and modified from the keypad and the optional configuration program, the Control System Toolbox.

The drawings in this section are function block diagrams for a typical Innovation Series Low Voltage drive. Refer to Chapter 2 for more detailed description of these functions.



Caution

To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify any programmable machine.

Note These diagrams are available as navigable, online drawings in the optional Windows®-based drive configuration software, the GE Control System Toolbox.

Diagram Title	Page Name
PWM Source–Control Overview	Overview
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Digital Inputs/Outputs & Mapping.....	HWIO_Dig
Analog Inputs/Outputs & Mapping.....	HWIO_Ana
Sequencing Overview.....	Ovr_Seq
General Sequencing.....	Gen_Seq1
Power Circuit & Charge Sequencing.....	Gen_Seq2
Phase Lock Loop and Regulator Enable/Run Sequencing.....	Gen_Seq3
Voltage Reference.....	Ovr_Ref_Sel

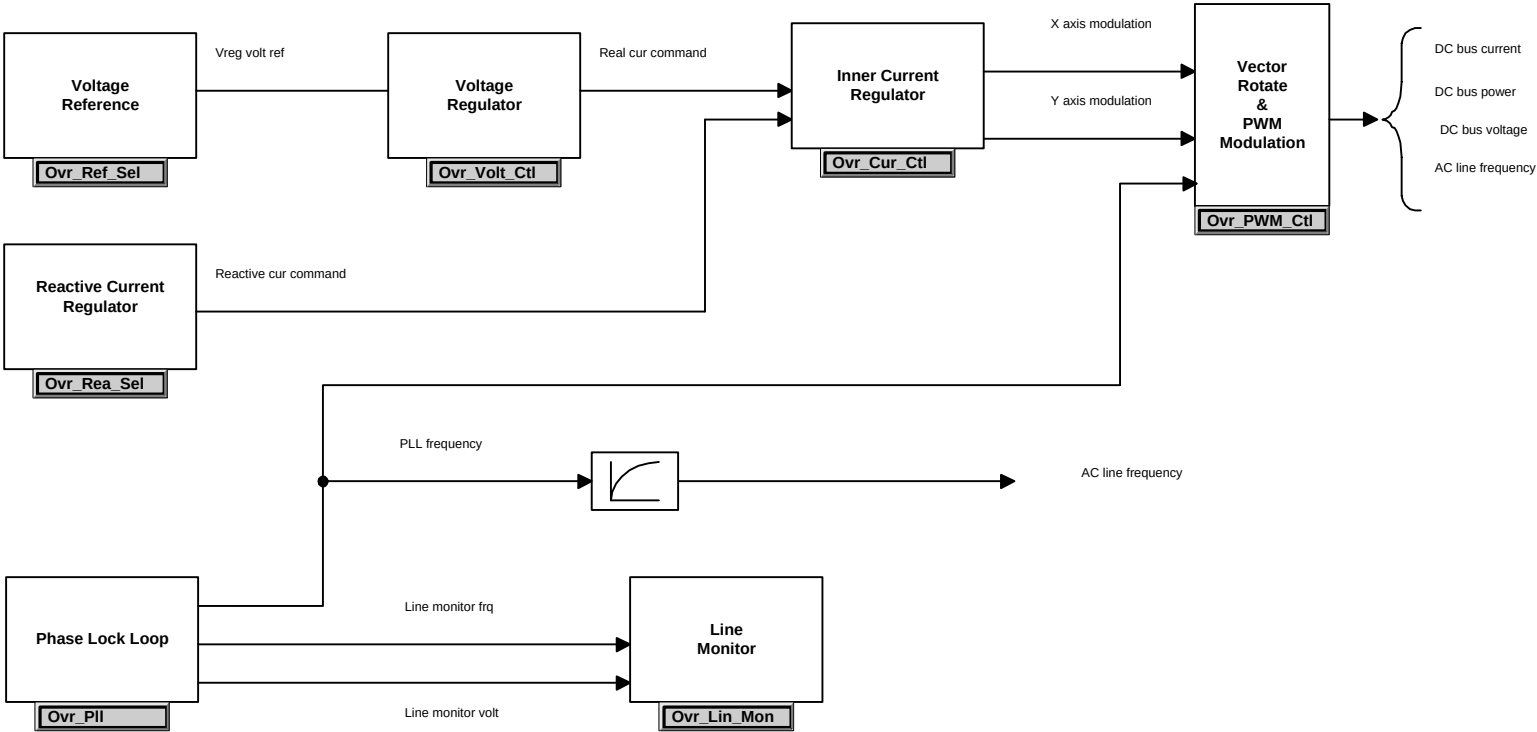
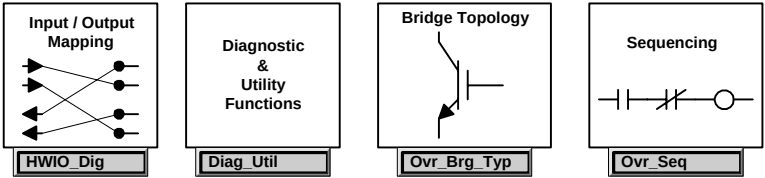
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Voltage Regulator.....	Ovr_Volt_Ctl
Inner Current Regulator.....	Ovr_Cur_Ctl
Vector Rotate & PWM Modulation.....	Ovr_PWM_Ctl
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NAVIGATION

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PWM Source - Control Overview



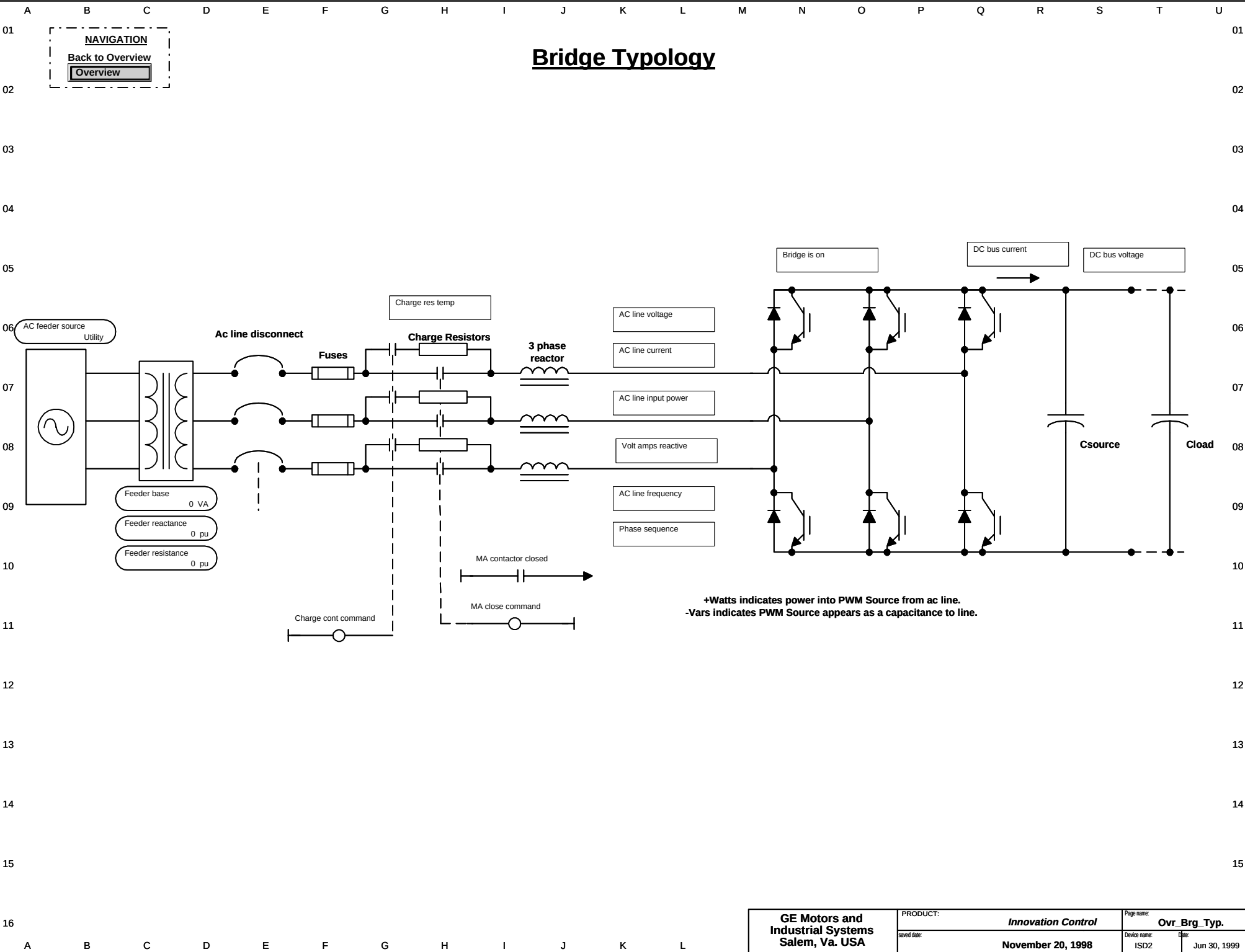
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- 6) **Sequencing Overview** ➔ **Ovr_Seq**
- 7) **General Sequencing #1 - Start / Stop** ➔ **Gen_Seq1**
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- 9) **General Sequencing #3 - Regulator Enable** ➔ **Gen_Seq3**

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17)	Capture Buffer Configuration	Capture
18)	Regulator Limit Diagnostics	Ovr_Reg_Lim

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Analog and Digital I/O Testing..... HWIO_Tst



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Page name: **Ovr_Brg_Typ.**
Device name: ISD2
Date: Jun 30, 1999

Digital Inputs/Outputs & Mapping

NAVIGATION

- Overview
- Analog I/O
- HWIO_Ana

Digital Inputs

ATBA Pin	Signal	Description
14	1+	Digital input 1
16	1-	Digital in 1 filter
18	2+	Digital input 2
20	2-	Digital in 2 filter
22	3+	Digital input 3
24	3-	Digital in 3 filter
26	4+	Digital input 4
28	4-	Digital in 4 filter
30	5+	Digital input 5
32	5-	Digital in 5 filter
34	6+	Digital input 6
36	6-	Digital in 6 filter

Dedicated Digital Inputs

ATBA Pin	Signal	Description
7	MA+	MA feedback
9	MA-	MA contactor closed

Sequencing Selectors

Fault Reset

- Fault reset select
- Unused boolean

Faults

- Xfrm OT fault sel
- User NC fault sel
- User NO fault sel

Run Command

- Hardware run ptr
- Digital input 1

Relay Outputs

ATBA Pin	Signal	Description
15	R1NO	Relay 1 state
17	R1COM	Relay 1 state
19	R1NC	Relay 1 state
21	R2NO	Relay 2 state
23	R2COM	Relay 2 state
25	R2NC	Relay 2 state
27	R3NO	Relay 3 state
29	R3COM	Relay 3 state
31	R3NC	Relay 3 state
11	SSRP	Solid state relay

Dedicated Relay Outputs

MB Pilot Relay

- Charge cont command
- Logic

MA Pilot Relay

- MA close command
- Logic

To Bridge Enable

- P5

System Fault String

ATBA Pin	Signal	Description
2	S115V	SYSTEM FAULT
4	S24V	SYSTEM FAULT
6	SCOM	SYSTEM FAULT
8	L115V	LOCAL FAULT
10	L24V	LOCAL FAULT
12	LCOM	LOCAL FAULT

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Date: Jun 30, 1999

Analog Inputs/Outputs & Mapping

NAVIGATION

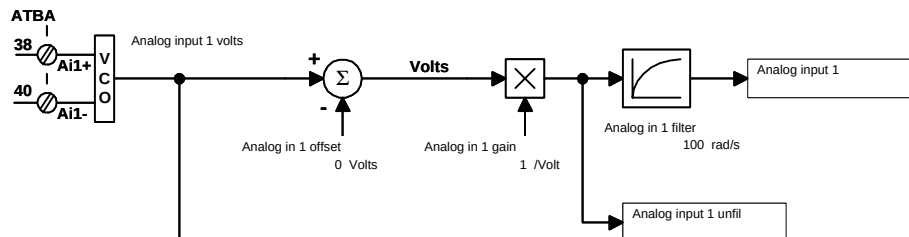
Overview

Digital I/O

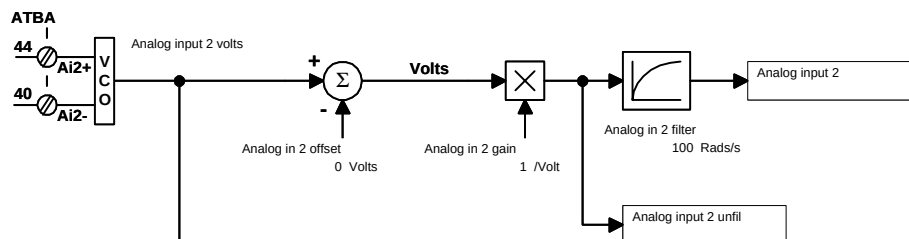
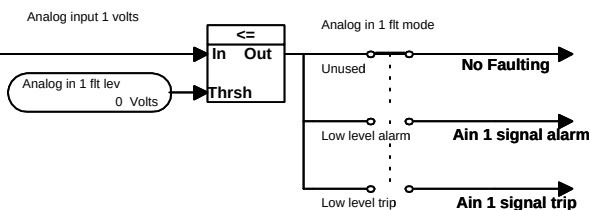
Overview

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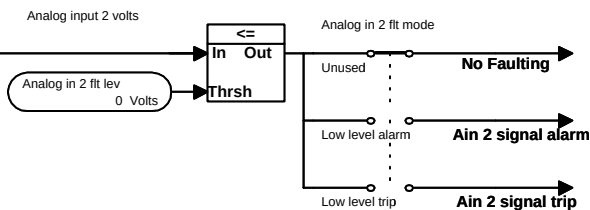
Analog Inputs



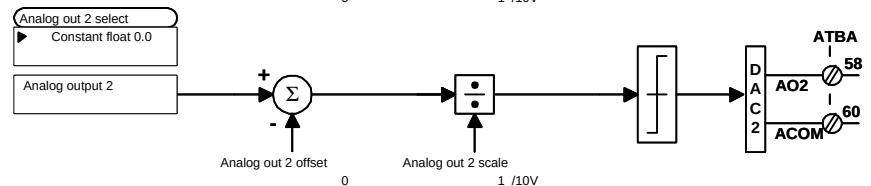
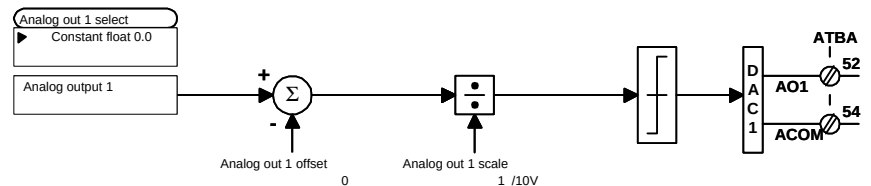
Loss of 4-20mA Protection



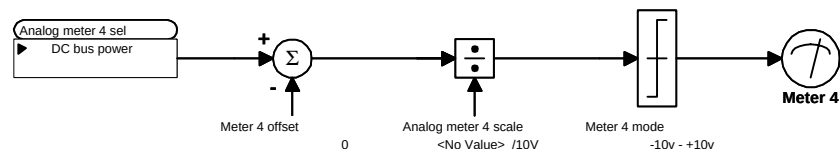
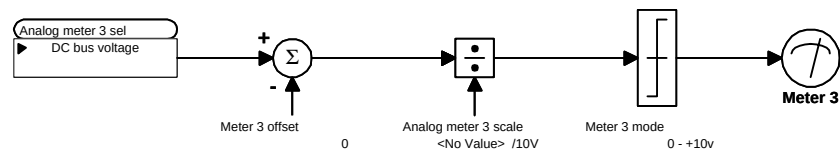
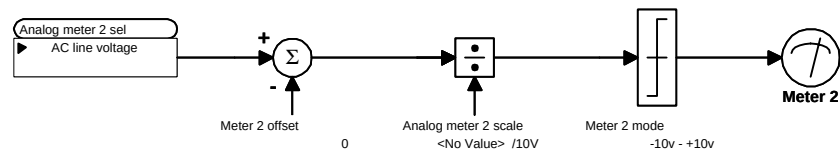
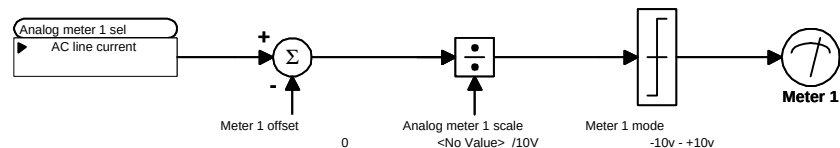
Loss of 4-20mA Protection



Analog Outputs



Meter Outputs



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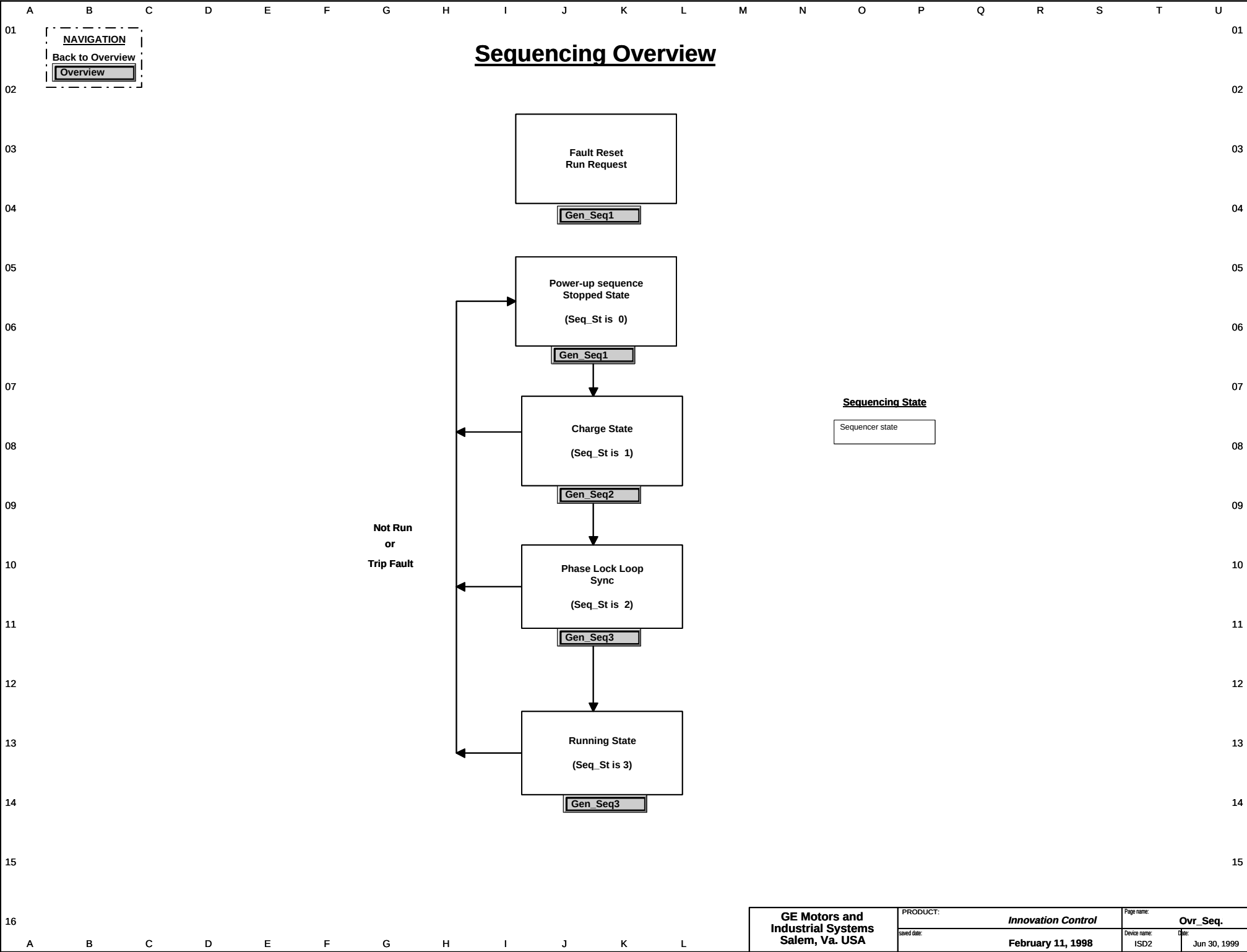
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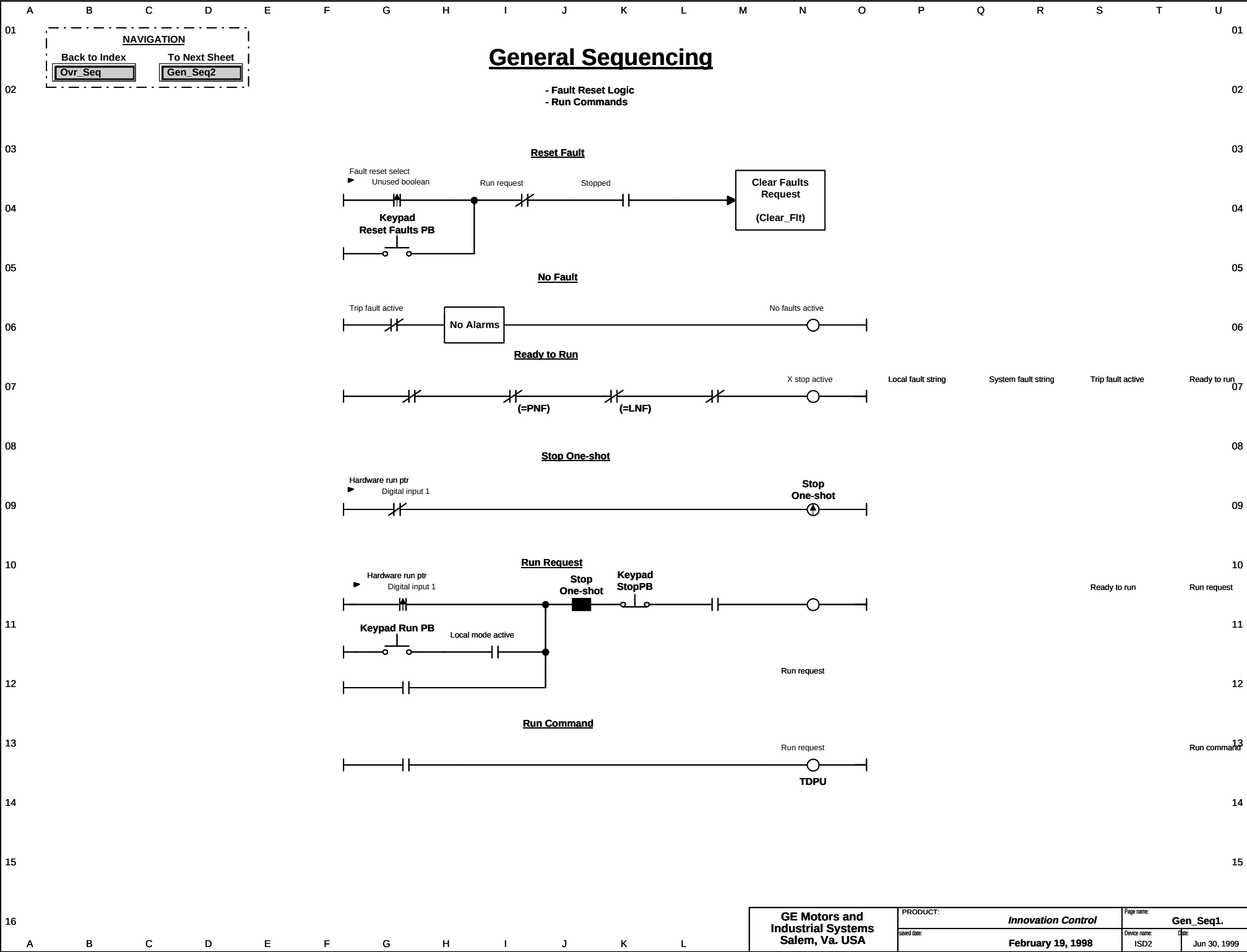
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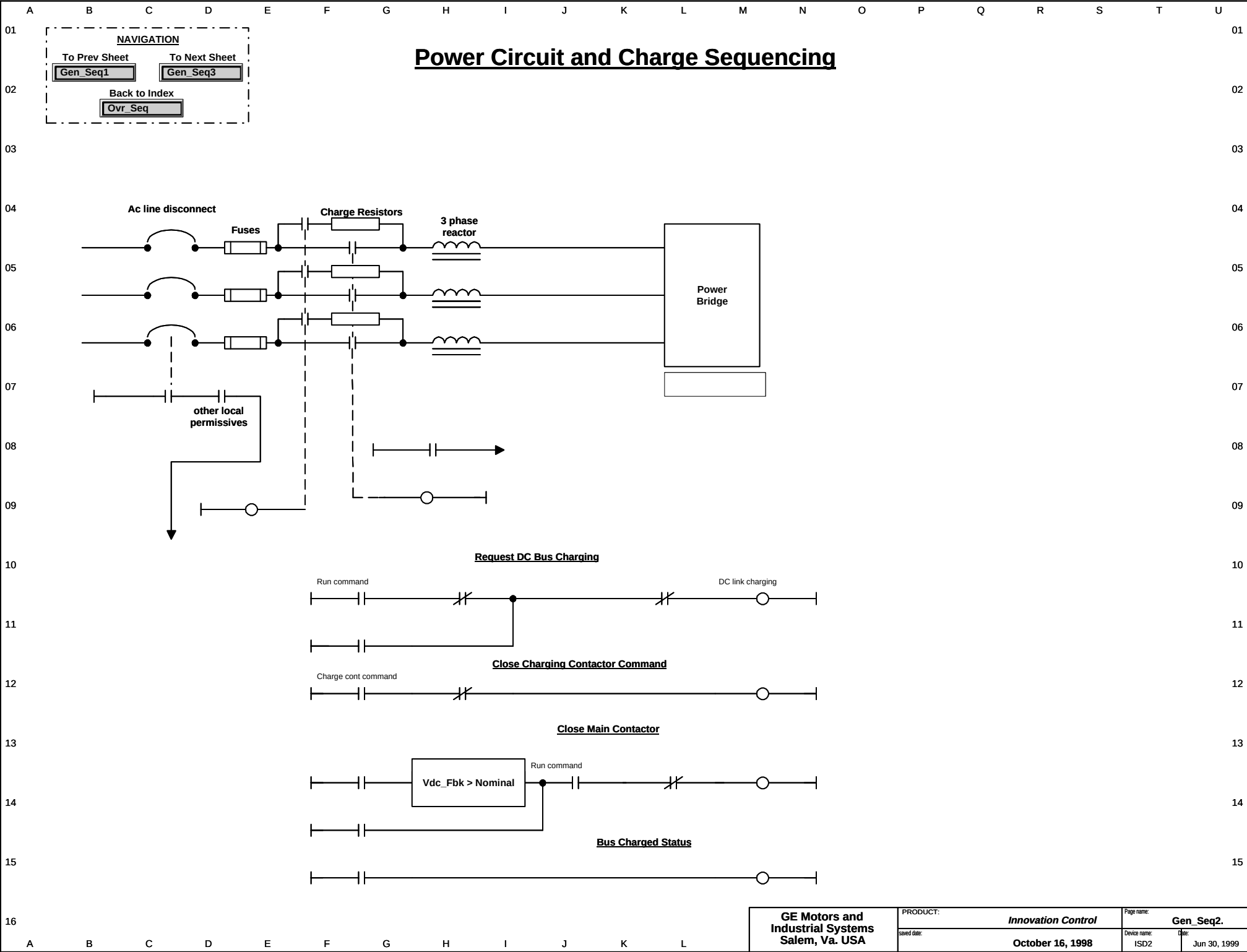
ISD2

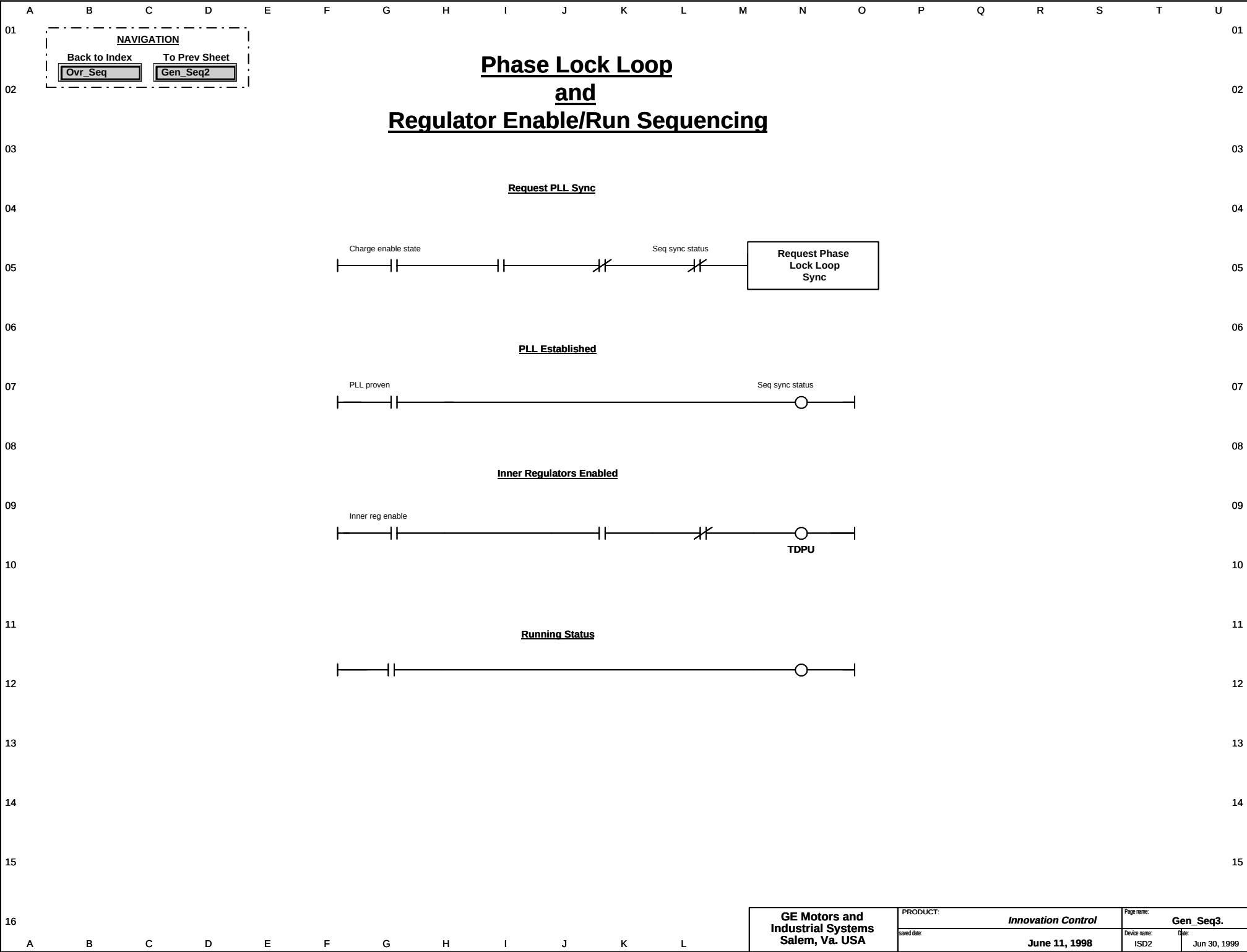
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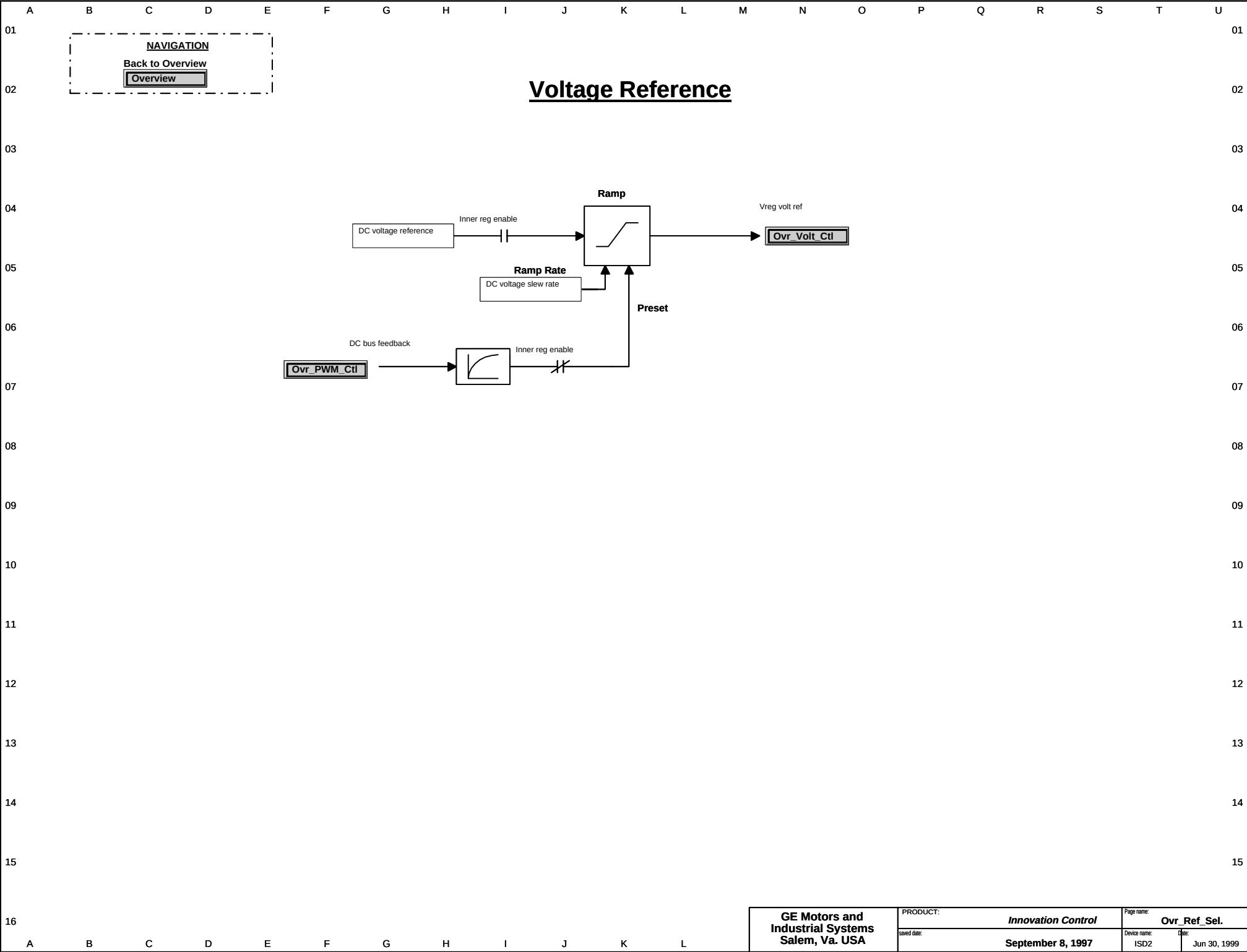
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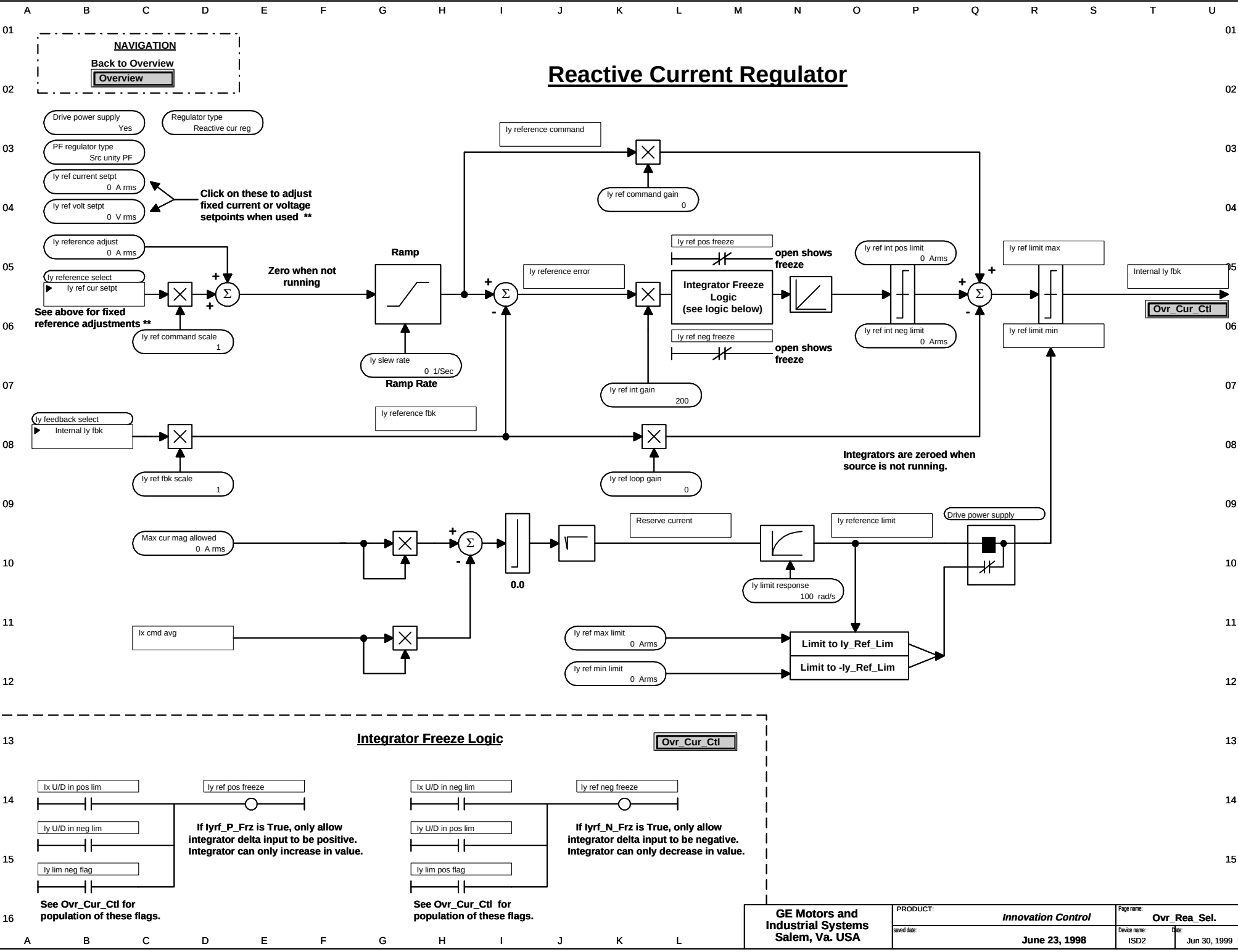


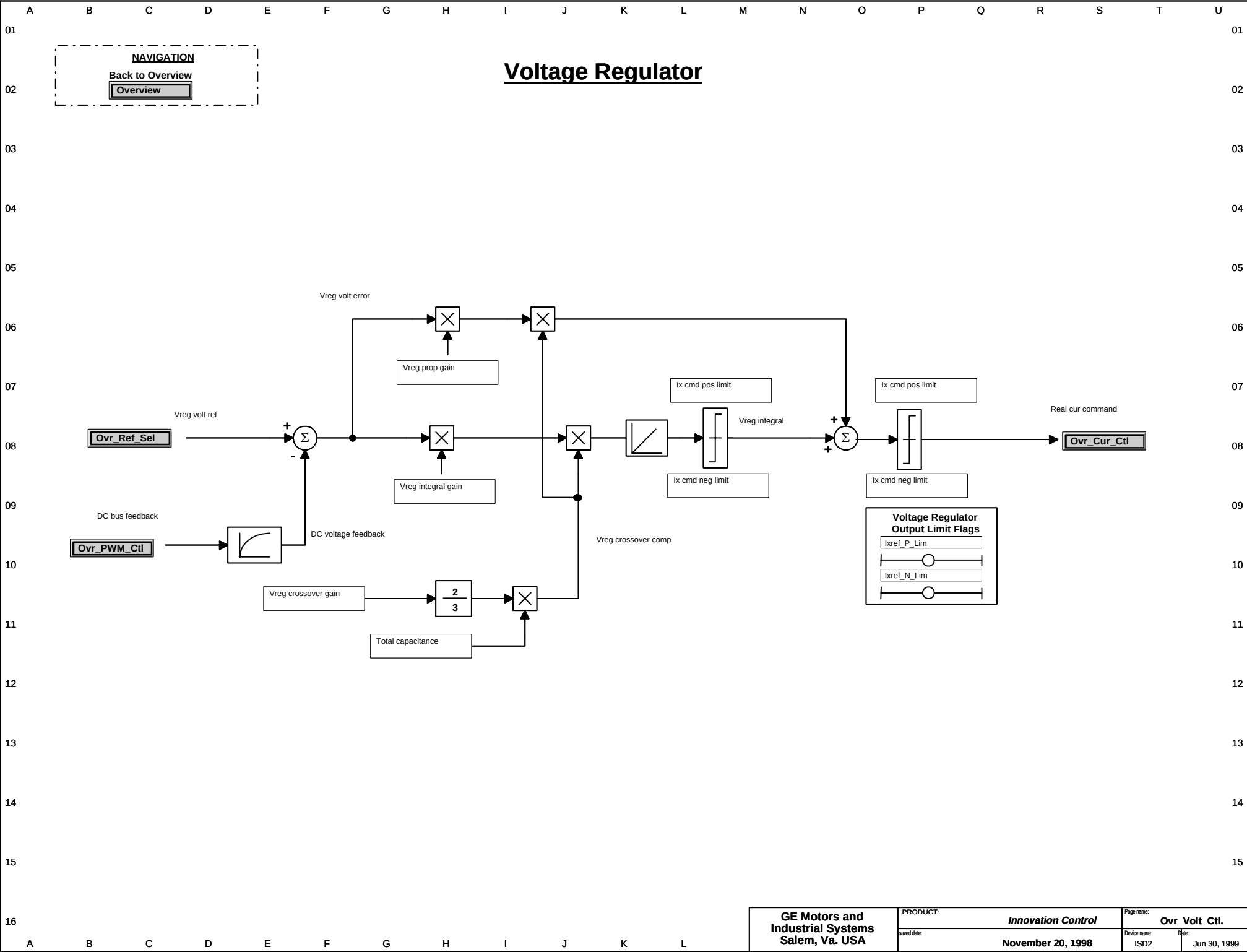










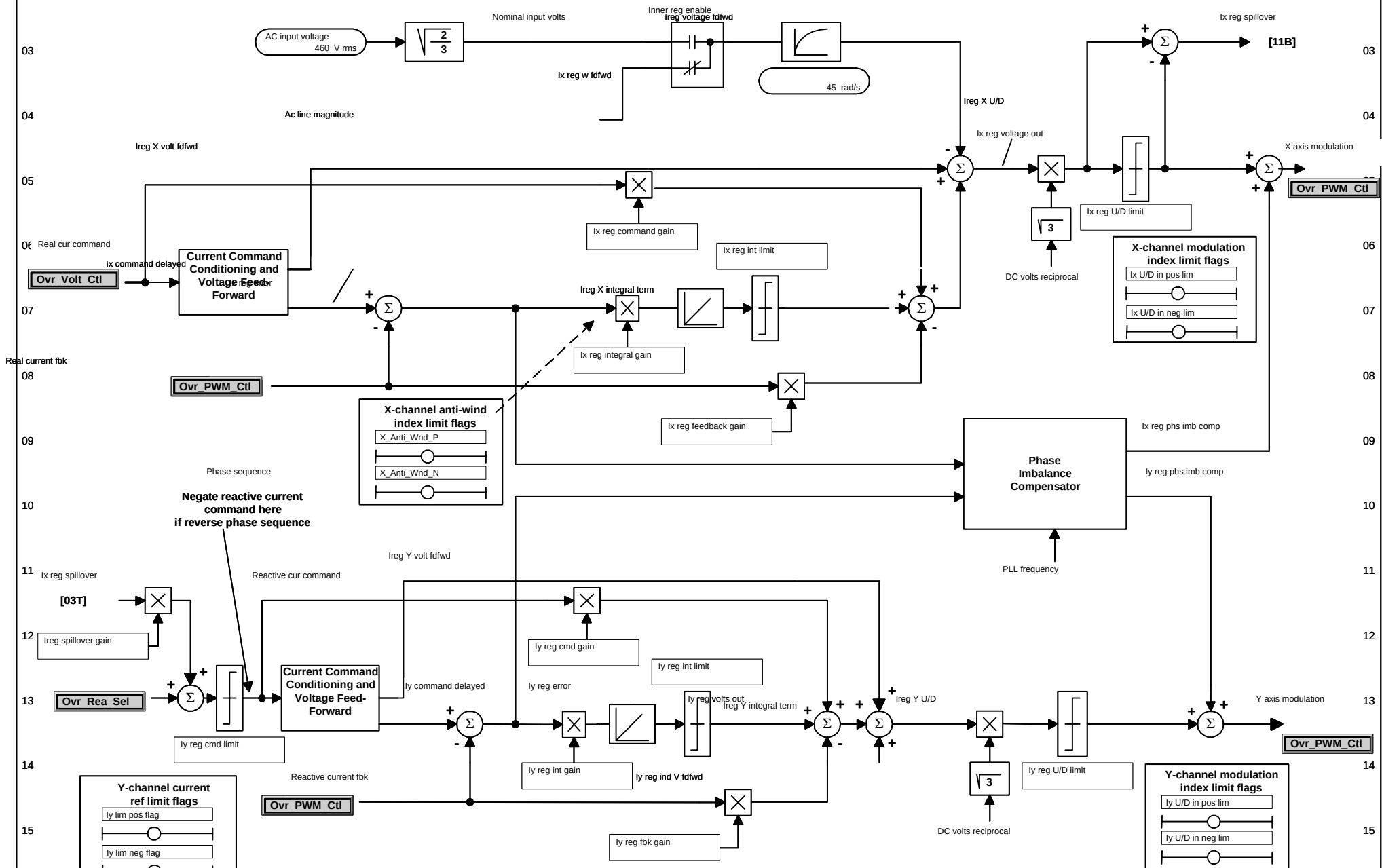


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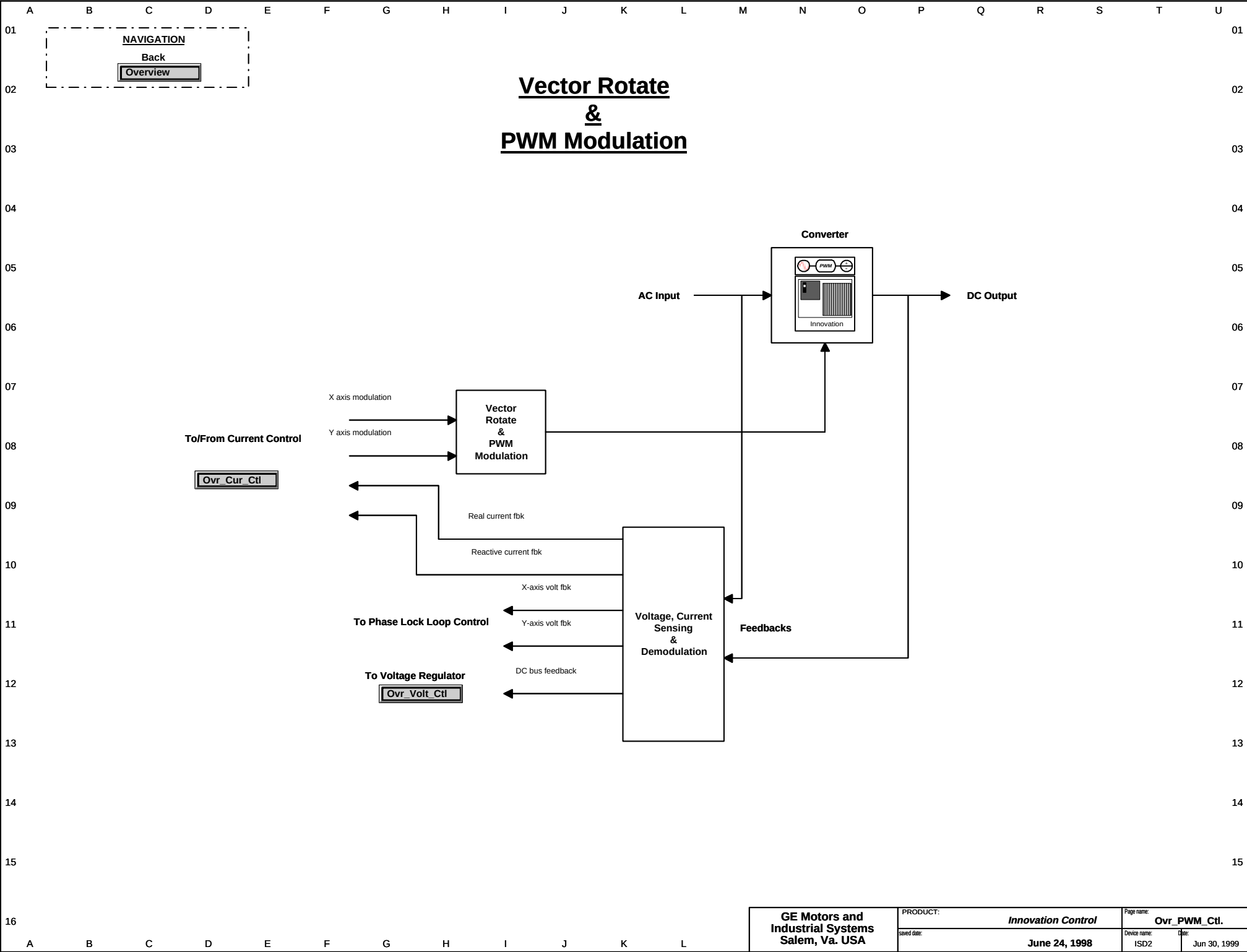
Inner Current Regulator

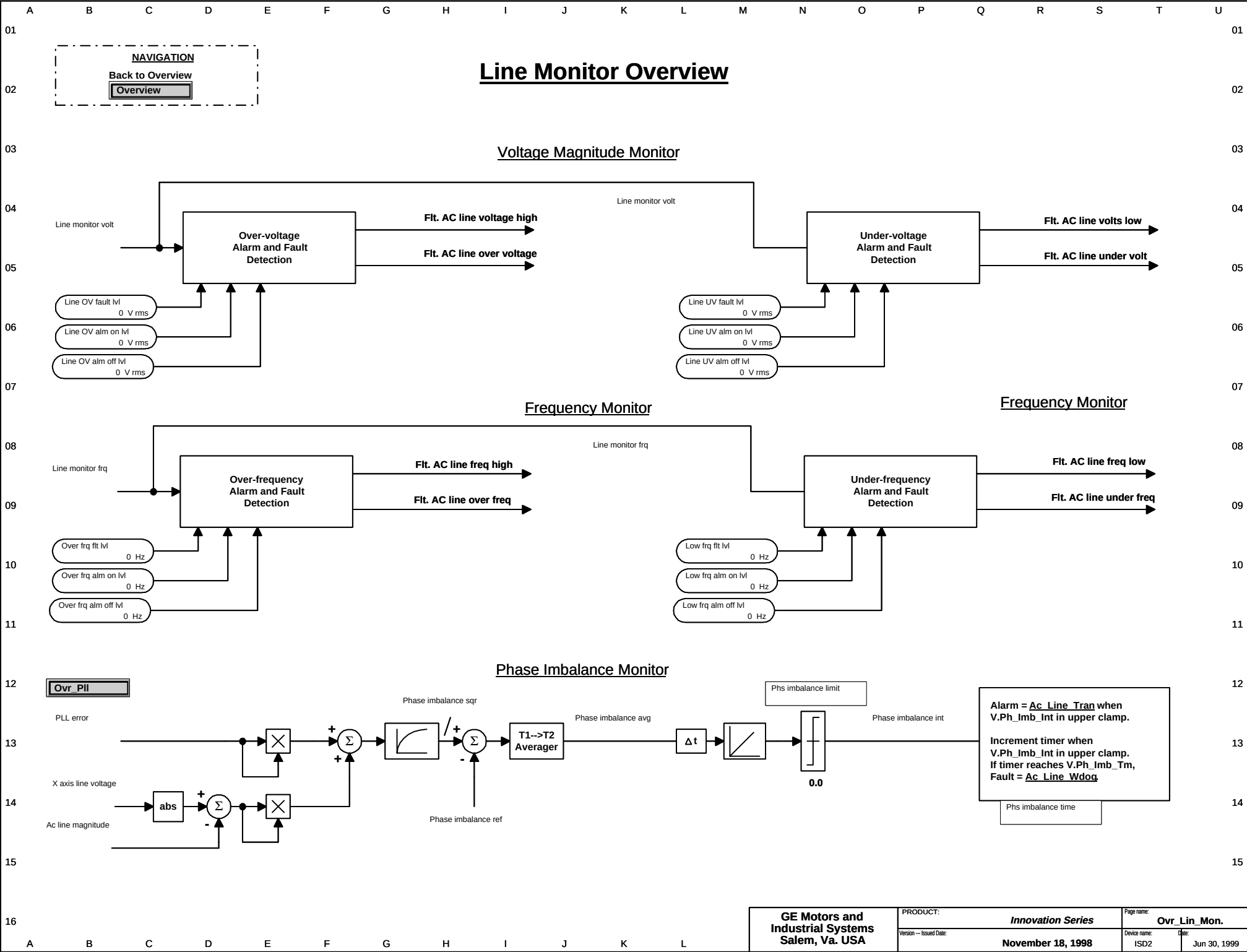


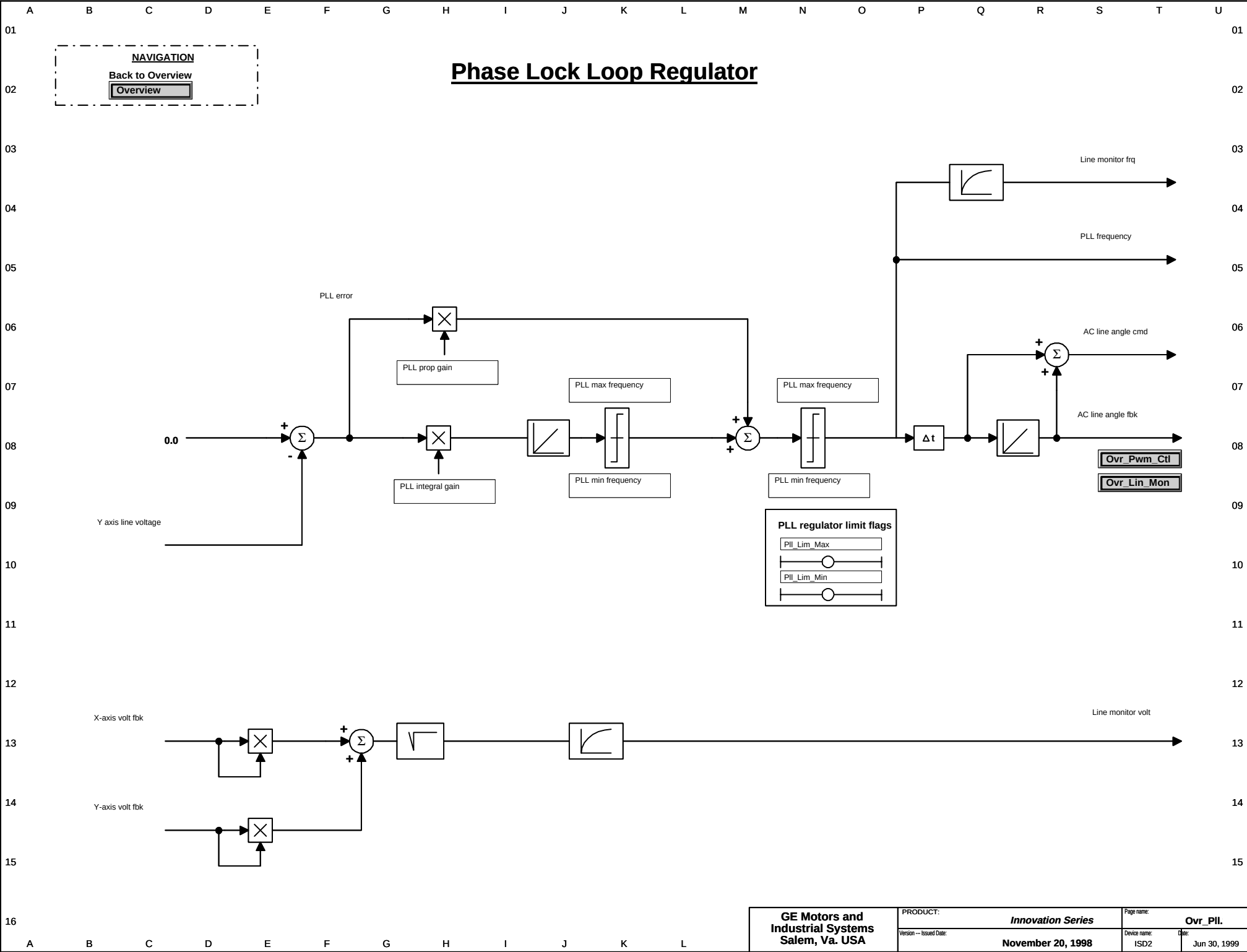
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Page name: **Ovr_Cur_Ctl.**
Device name: **ISD2**
Date: **Jun 30, 1999**



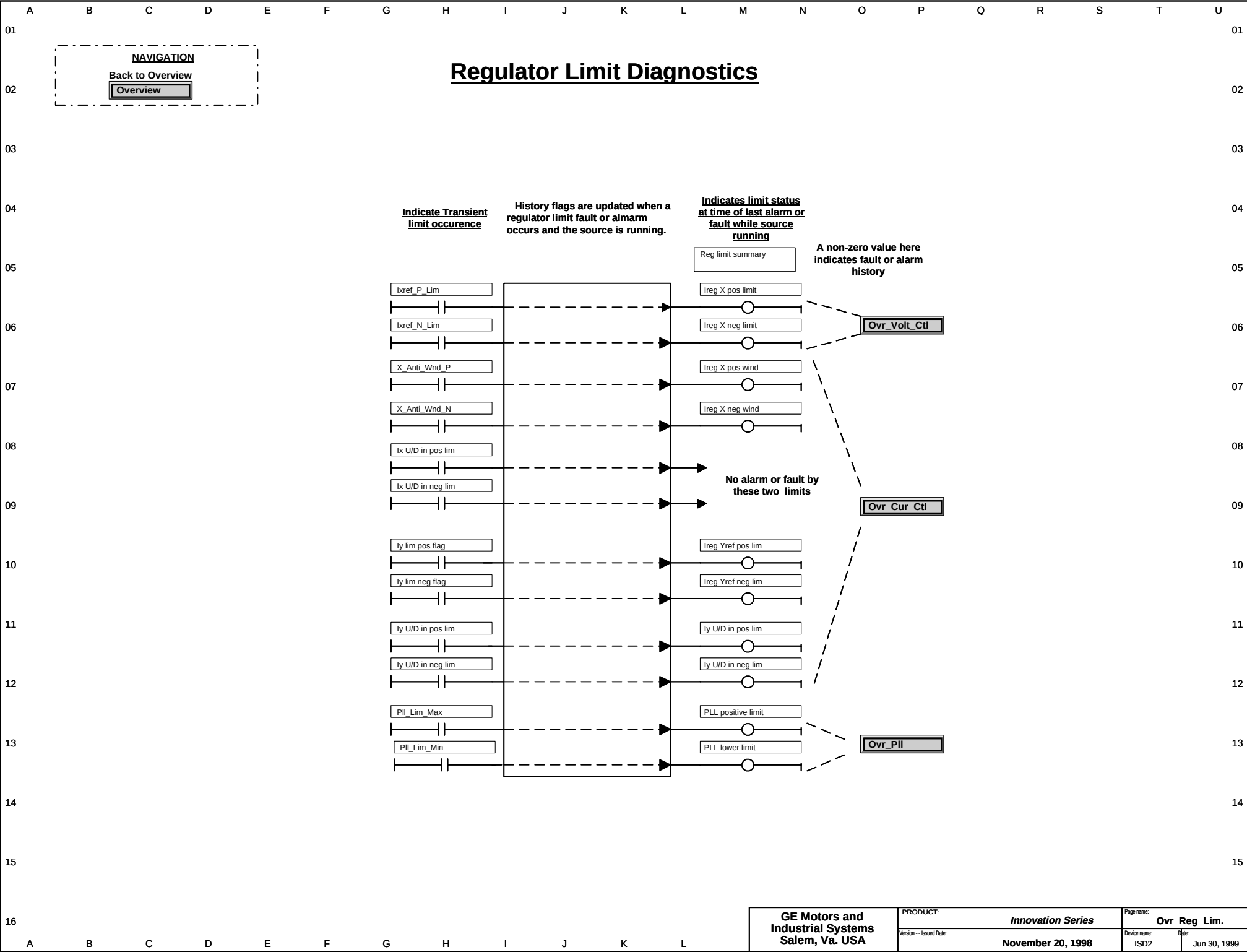


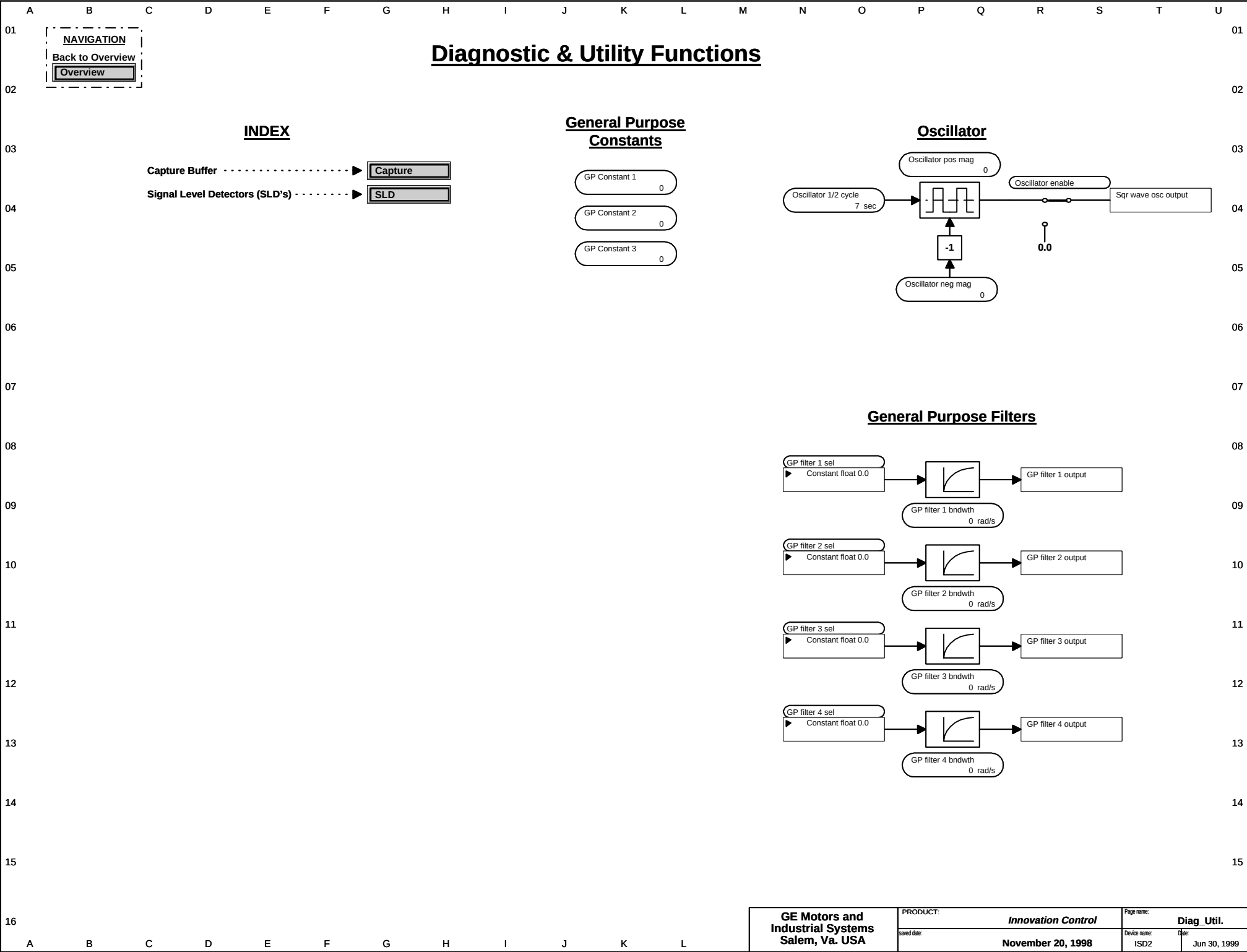


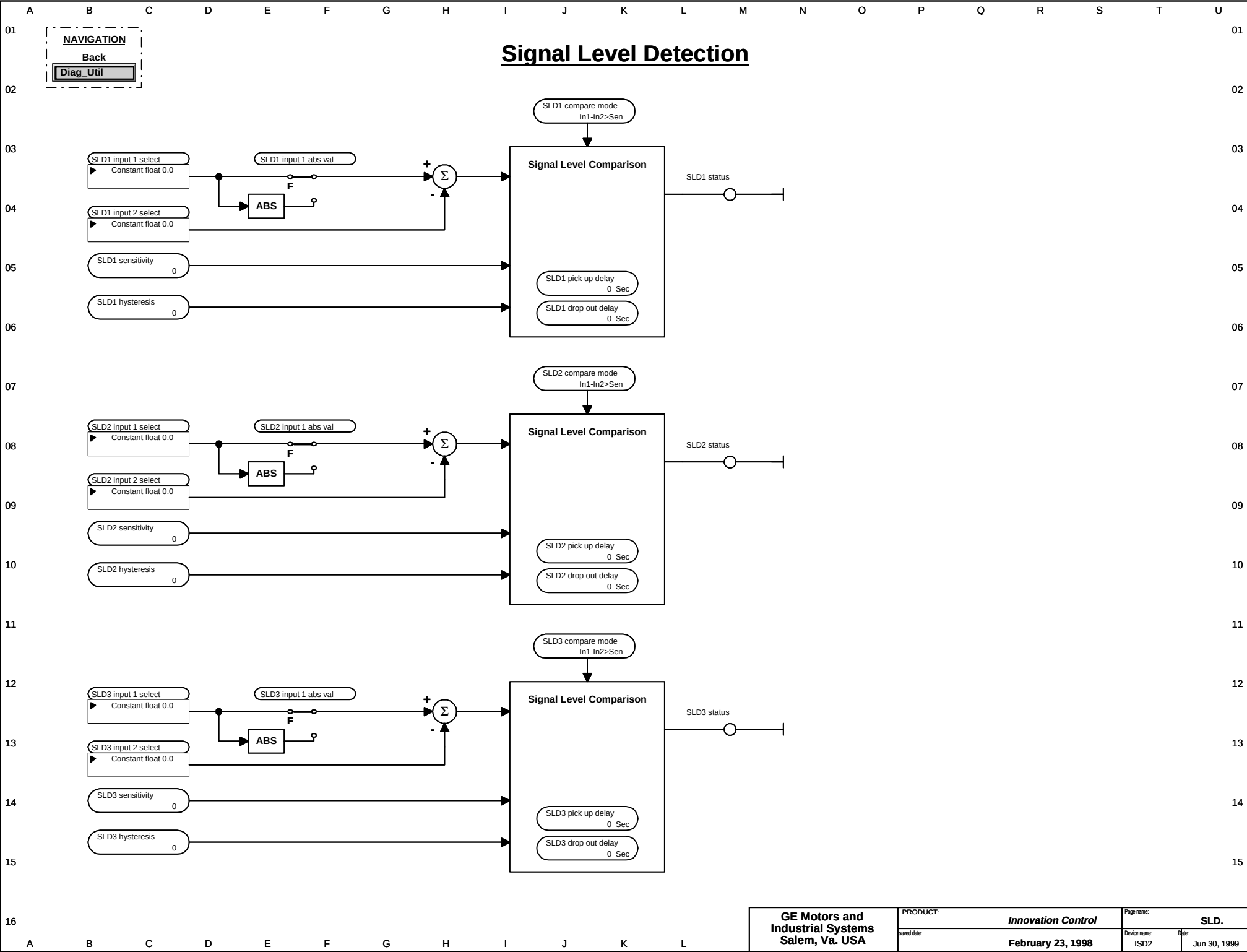
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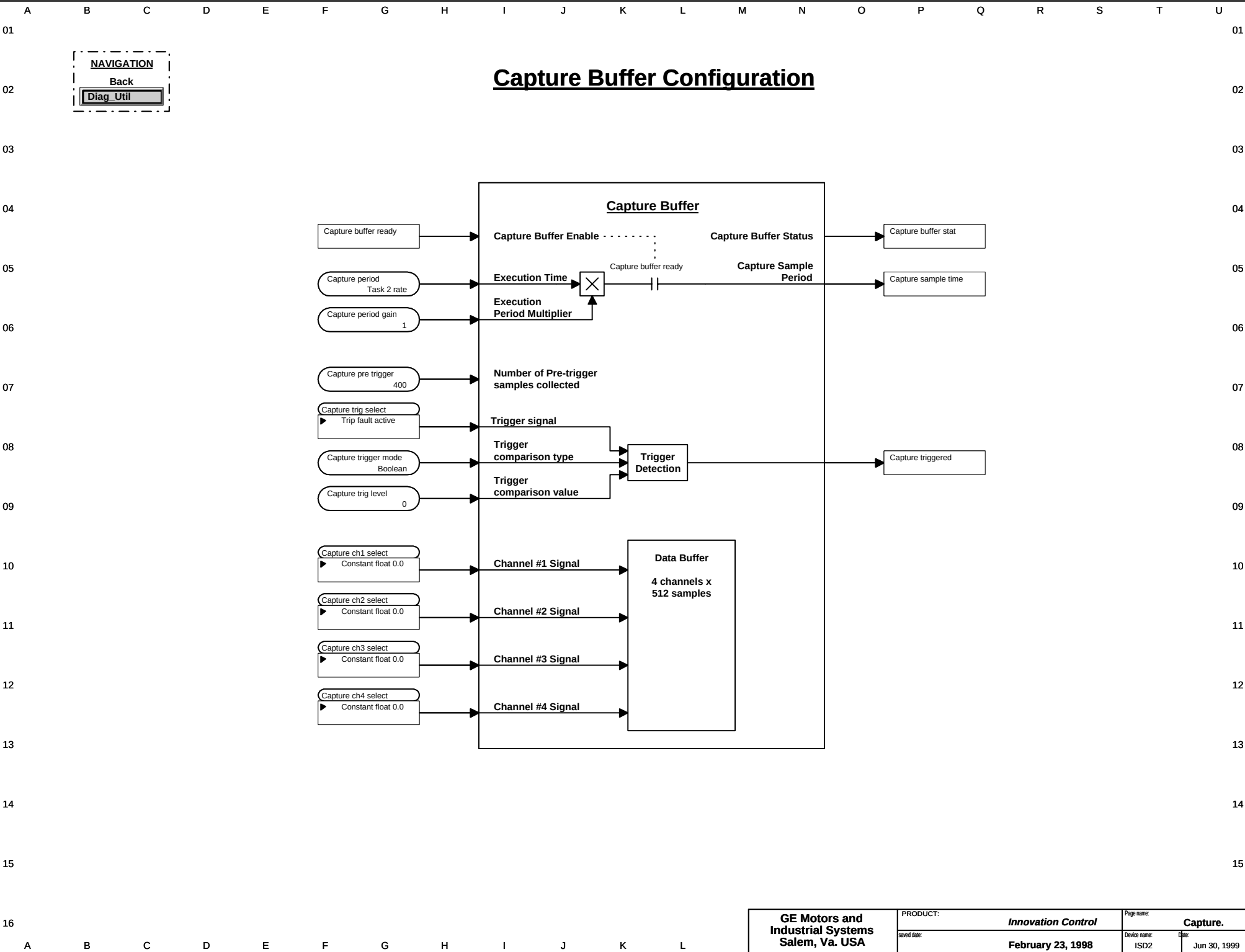
Pll_Lim_Max

Pll_Lim_Min

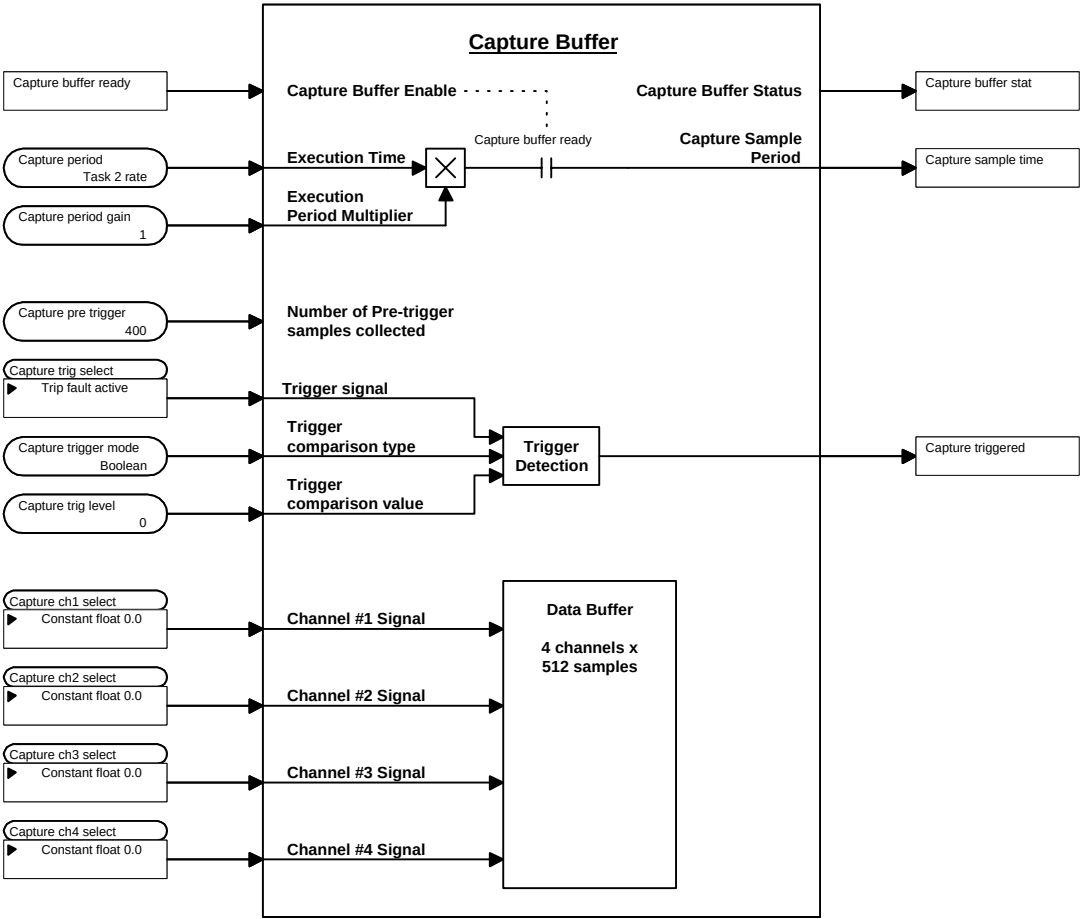








Capture Buffer Configuration



Glossary of Terms

ACCBN

AC product, Common Bus Non-regenerative source. This source provides dc power to a dc fed, ac product (such as ACDCF), and is not capable of regenerating power to the ac line.

ACCBR

AC product, Common Bus Regenerative source. This source provides dc power to a dc fed, ac product (such as ACDCF), and is capable of regenerating power to the ac line.

ACDCF

AC product, DC Fed inverter. This inverter is powered from a source bridge (such as ACCBN, ACCBR).

drive

(Industrial.) The equipment used for converting available power into mechanical power suitable for operation of a machine.

filter

An electrical circuit that passes frequencies within a specified frequency band and attenuates signals that fall outside of that frequency band. (Also see line filter, ac.)

frame

Size of drive cabinet(s). Determined by hardware components required for power application.

harmonic distortion

Undesired harmonic frequencies that result from irregularities in a transmission line.

layout drawing

A diagram showing the components of a panel, and their location and connections.

line filter

A filter that connects from ac line to ac line at the input of a power converter. The filter consists of a series configuration of resistors and capacitors, which damps out high frequency oscillations on the ac power line.

NEMA

National Electrical Manufacturers Association. An organization that develops standards for the electrical manufacturing industry.

non-regenerative

See regenerative.

outline drawings

A drawing or diagram that shows the dimensions and non-detailed layout of a device or equipment.

parameters

Used in the drive for configuration of functions. For example, six parameters are used to configure the ramp rate function generator in the general industries pattern.

reactor

A device (such as a coil, winding, or conductor of small resistance) used to introduce reactance into an alternating-current circuit.

regenerative

Ability of a drive to return power from the motor armature to the ac line. Creates a braking effect on the motor.

signals

LAN or I/O based variables that either control the drive or provide feedback data on the status of the drive. For example, an analog input signal provides the speed reference for the drive.

variables

Dynamic references for control of the drive or contain feedback on the status of the drive. For example, speed feedback and speed reference are two variables associated with the speed regulator function in the drive.

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