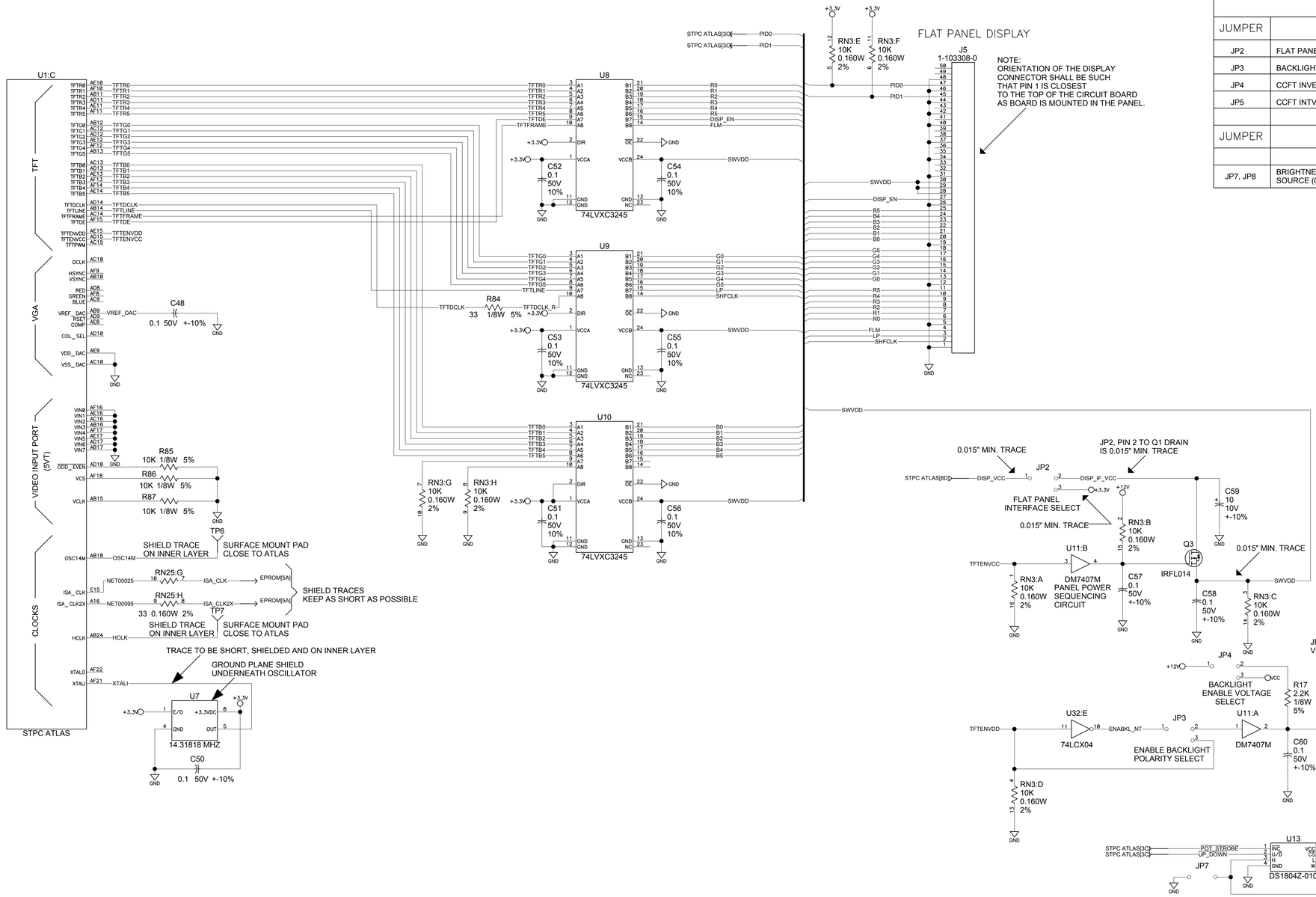

DISPLAY INTERFACE JUMPER SETTINGS		
JUMPER	PINS 1–2	PINS 2–3
JP2	FLAT PANEL POWER AND LOGIC LEVELS = +5 VDC	FLAT PANEL POWER AND LOGIC LEVELS = +3.3 VDC
JP3	BACKLIGHT ENABLE SIGNAL POLARITY LOW. (INVERTED)	BACKLIGHT ENABLE SIGNAL POLARITY HIGH. (NOT INVERTED)
JP4	CCFT INVERTER LOGIC LEVEL = +12 VDC	CCFT INVERTER LOGIC LEVEL = +5 VDC
JP5	CCFT INTVERTER POWER = +12 VDC	CCFT INVERTER POWER = +5 VDC
JUMPER	IN	OUT
JP7, JP8	BRIGHTNESS CONTROL REQUIRES VARIABLE VOLTAGE SOURCE (0-2.2V)	BRIGHTNESS CONTROL REQUIRES VARIABLE RESISTANCE ONLY

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE IN MICROFARADS;
   ALL RESISTORS ARE IN OHMS
2. COMPONENTS WITH GATES THE:
   POWER PIN IS CONNECTED TO NET VCC OR +3.3V.
   GROUND PIN IS CONNECTED TO NET GND.

REV. LEV.	DATE	REVISION RECORD	CHG. NO.	DR.	CK.
–		NEW.	NOT REL'D	KAW	BAS
A	04-03-03	SEE OTHER SHEETS.	0702-0007	KAW	BAS
B	10-17-03	SEE SHEET 7.	0703-3024	KAW	BAS

"ALL PROPRIETARY RIGHTS IN THE SUBJECT MATTER HEREOF ARE RESERVED, AND NO PERMISSION IS GRANTED TO REPRODUCE THIS PRINT IN WHOLE OR IN PART, OR DISCLOSE ANY OF THE INFORMATION UPON IT TO OTHERS WITHOUT WRITTEN RELEASE BY YORK INTERNATIONAL CORPORATION."

YORK INTERNATIONAL CORPORATION

YORK, PA 17405

DIMESNIONS ARE IN INCHES
DO NOT SCALE
TOLERANCES PER ENG. STD. M-282
WELDING PER ENG. STD. M-30
REF. DWG.

CONTROL,
OPTIVIEW MICROPROCESSOR BOARD,
DISPLAY INTERFACE SCHEMATIC
(REF. DWG.)

MATERIAL
TYPE _____ ENG. STD. E-355
PART NO. _____
CUT SIZE _____

NAME	DATE
DR. K. A. WERTMAN	04-15-02
APPR. B. A. SMITH	05-15-02
SCALE: N.T.S.	

SIZE	CAGE NO	DRAWING NUMBER
D	66935	031-02430-999

Tue Nov 25, 2003 | WT.= LBS. | ORIG. NO. | SHEET 2 OF 9

031-02430-999_b0.sch